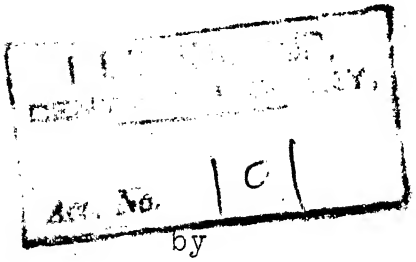
DESIGN OF A COINCIDENT CURRENT MEMORY SYSTEM

A Thesis submitted

in partial fulfilment of the requirements

for the degree of

Master of Technology



by

VICKRAM SONDHI

to the

Department of Electrical Engineering

Indian Institute of Technology

Kanpur

July 1968

This is to certify that this work on DESIGN OF A COINCIDENT CURRENT MEMORY SYSTEM has been carried out under my supervision and it has not been submitted elsewhere for a degree.

H.N. Mahabala

Dr. H.N. MAHABALA
Assistant Professor
Department of Electrical Engineering
Indian Institute of Technology
Kanpur.

A C K N O W L E D G E M E N T

I am grateful to Dr. H. N. Mahabala for his constant help and guidance during the Project work.

I wish to thank Dr. V. Rajaraman for his valuable suggestions and Dr. T. R. Vishwanathan and Professor D. L. Stephenson for their help in the design of the Electronic circuits.

No less thanks are due to the Staff of the Electrical Engineering Department and my colleagues for their forbearance.

S_Y_N_O_P_S_I_S

The recent appearance of low level switching and core driver transistors and magnetic cores has made an indigenous Memory System a feasible proposition.

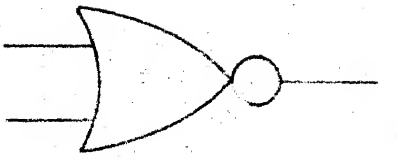
The necessary driving, selection and sensing circuits for a 256 word memory having a cycle time of 10 microseconds have been designed and tested. In addition, the complete system design including the Timing Generator is discussed in some detail.

TABLE OF CONTENTS

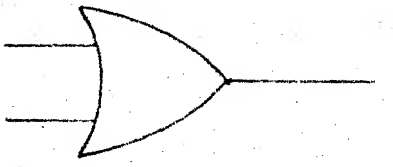
CHAPTER PAGE

....

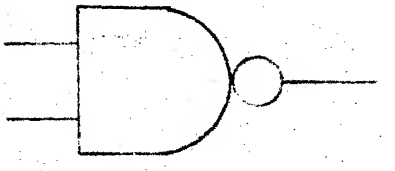
LOGIC SYMBOLS



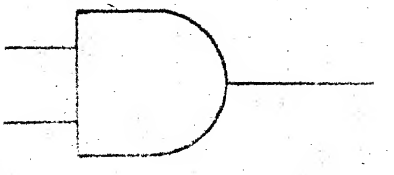
NOR



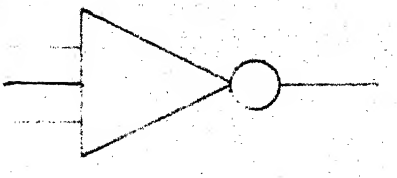
OR



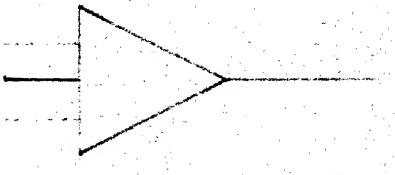
N AND



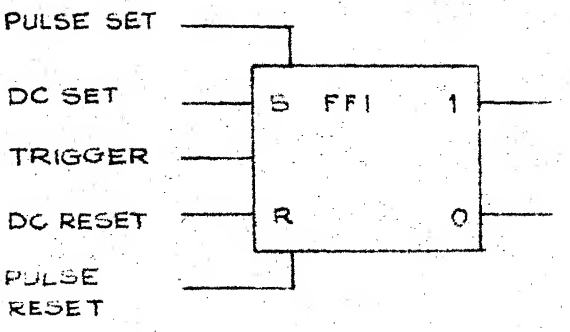
AND



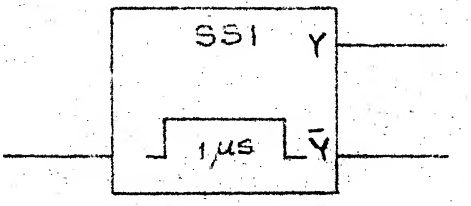
INVERTING
AMPLIFIER



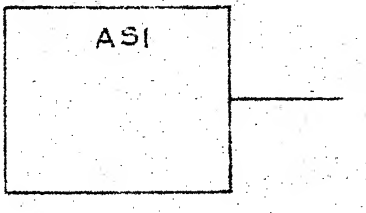
NON-INVERTING
AMPLIFIER



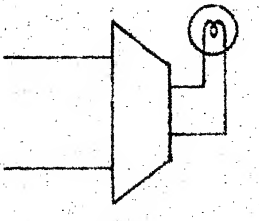
FLIP FLOP



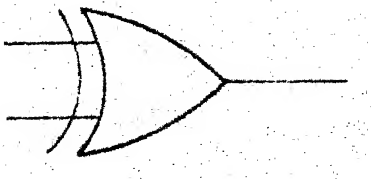
MONOSTABLE MULTIVIBRATOR



ASTABLE MULTIVIBRATOR



LAMP DRIVER



EXCLUSIVE OR

CHAPTER I

I_N_T_R_O_D_U_C_T_I_O_N

The ability to store large amounts of information and access it rapidly is one of the main factors that makes digital computers powerful. The desirable features of a memory are :

(i) Low power consumption.

(ii) Operating speed compatible with speed of control and arithmetic units.

(iii) Reliable operation.

(iv) Compactness.

(v) Ease of fabrication.

(vi) Low cost.

All these characteristics are not compatible and the main problems in memory design consist of arriving at an optimum design.

Since its conception in 1951, the magnetic core memory has established itself as a very attractive memory device for digital computers. Among its virtues are excellent reliability, capability of high speed operation, and capability of large storage capacity in compact size. In all modern digital computers information is represented in the binary code. By its very nature, this code requires a large number of binary digits to represent a single number. The storage capacity of a digital computer may thus run into many thousands of bits and consequently

the cost factor becomes important. With the improved methods of manufacture it is now possible to produce very cheap and yet extremely reliable magnetic cores.

Announcement of the digital magnetic element followed that of the transistor by about eighteen months. This made possible the realisation of an all solid state memory system in which the associated circuits were compatible with the core storage arrayin reliability, speed, compactness, and power consumption. A large effort has been spent by the electronics industry in developing transistor devices suitable for memory applications. The result has been the present day availability of transistors which can switch several hundred milliamperes of current in a fraction of a microsecond. In addition, extensive experience and recent developments in magnetic cores have made realisable memory systems with a cycle time approaching half a microsecond. The requirement for mass fabrication and high speed operation has led to the development of the Thin film memory. However, perfection for large systems has not yet been attained and research in this field continues.

The fabrication of a memory system using indigenous components has been hampered by the nonavailability of suitable magnetic and transistor devices. The recent appearance of magnetic cores and switching transistors seem to indicate that a completely indigenous memory system may be realisable. Although the magnetic cores presently

available leave much to be desired in terms of output and switching time, they do show promise for use in memory systems with a cycle time of the order of ten microseconds.

The low level switching transistors currently available have shown exceptionally good qualities and logic circuits operating at speeds higher than 1 mc/s have been tested. In addition, PNP and NPN core driver transistors capable of switching half an ampere in less than a microsecond have also recently become available.

The present work was undertaken to investigate the possibility of developing a small memory system for an Educational Computer using indigenous components. Extensive tests were performed on available switching transistors and magnetic cores to ascertain their suitability for use in digital systems. The tests have shown that such systems are definitely feasible.

CHAPTER II

THE MAGNETIC CORE

Square loop properties are exhibited by many ferrite materials but the only materials in common use at the present time are ceramics with a cubic crystal structure and the general composition MFe_2O_4 where M is a divalent metal or mixture of metals such as Magnesium and Manganese.

The powdered ceramic is pressed into moulds of the required shape and sintered at around 1300°F until proper crystallisation has occurred. Crystal structure and uniformity of composition are important factors in obtaining a square hysteresis loop. Toroidal cores are most commonly used but other shapes such as multiaperature cores and ferrite plates are also made for special purposes. The two main properties which render such ferrites suitable for high speed storage and switching elements is their rectangular hysteresis loop and high resistivity. The value of the latter is greater than 10^5 ohms/cm. which makes the eddy current losses negligible.

2.1 The Low Frequency Hysteresis Loop :

A typical low frequency hysteresis loop of a square loop ferrite toroidal core is shown in Fig. 2.1. This graph is a plot of the flux density B vs the magnetic field H. As the field H is applied, the flux through the core reaches a maximum beyond which increasing H will not increase B. In this state the core is said to be saturated. If the field is

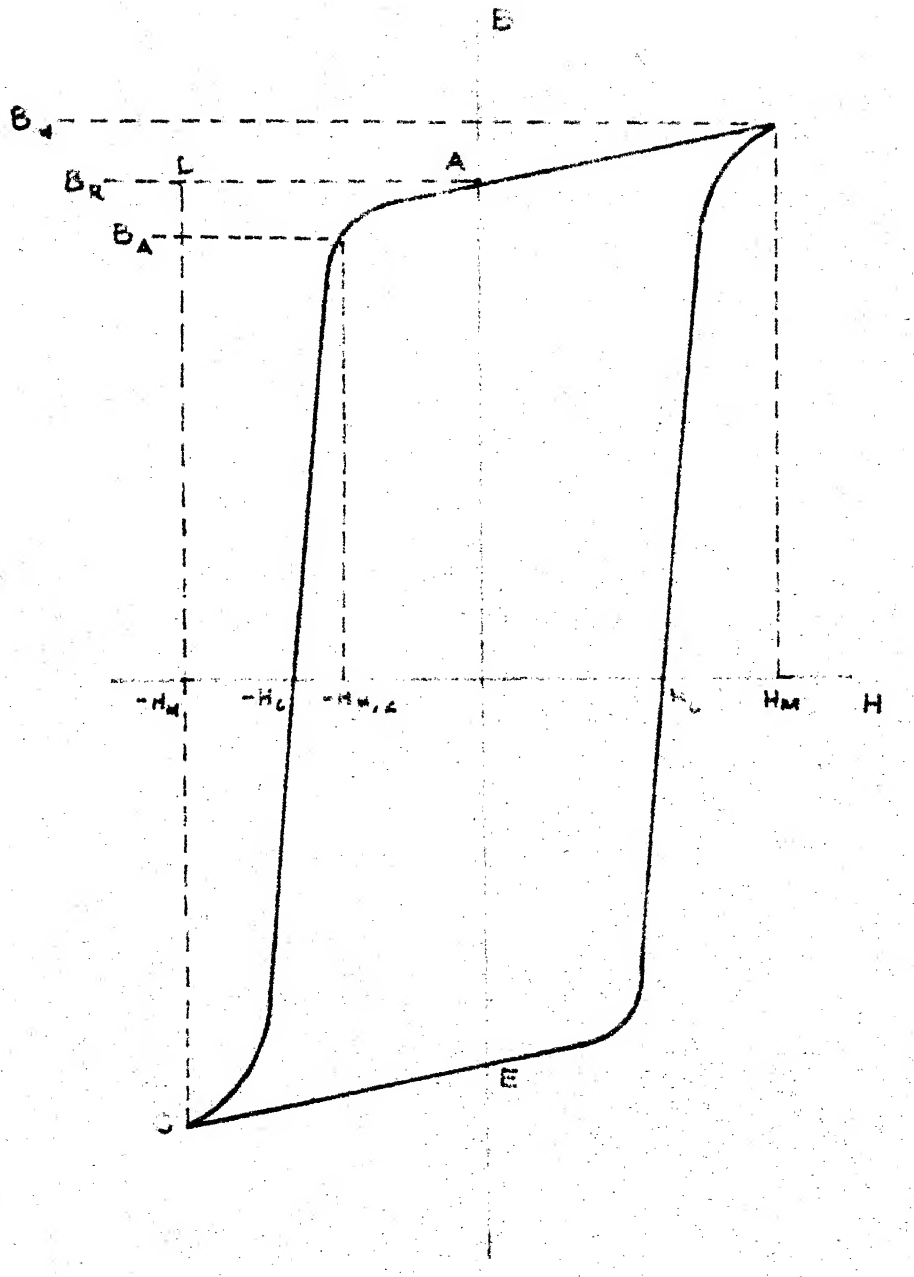


FIG 2.1 TYPICAL HYSTERESIS LOOP OF A SQUARE LOOP FERRITE CORE

now decreased to zero, the core will retain most of its flux. The flux density B_R, at this point is called the remanence or retentivity. If H is now reversed in direction the flux will suddenly drop rapidly. The magnitude of H for which B = 0 is called the coercivity or coercive force H_C. The direction of the flux density will now change and the core will again become saturated but in a sense onposite to the previous saturated state. Thus the core can have two distinct remanent states. The process of changing H so that the core goes from one remanent state to the other is referred to as switching of the core. Magnetic matrix stores usually use a coincident current drive selection where the main property is that, while a field H_M, is sufficient to switch the core from one remanent state to the other, a field $H_M/2$ is insufficient to cause any significant change of flux. Thus if B_M and B_A are the flux density levels produced by fields H_M and $H_M/2$, a figure of merit of the core when used in a coincidence drive system is the squareness ratio B_A/B_M. The maximum squareness ratio which usually exceeds 0.9 is achieved when a loop rather smaller than the saturation loop is employed.

It may be observed that when the core is in either one of the two stable states there is no expenditure of energy to maintain that state. Only when the core is taken from one stable state to another is energy expended. This observation is of great practical advantage as it implies that no power is needed to retain the device in a stable state.

Flux changes in the core may be reversible or irreversible. In a reversible flux change the core returns to its original state after the applied field is removed. A field which is not large enough to take the state of the core beyond the knee of the hysteresis loop produces mainly reversible changes. Larger applied fields result in permanent changes of flux and the core switches. If the applied field H_M is applied as a step change, the core will follow the path ADC, Fig. 2.1, rather than the path AC along the loop, and the e.m.f. generated in a wire linking the core will show two peaks. The first of these is due to reversible flux changes and the second to the irreversible ones which are much slower. This difference in speed arises from the difference in mechanism by which flux changes take place within the material.

2.2 Mechanism of Reversible and Irreversible Switching :

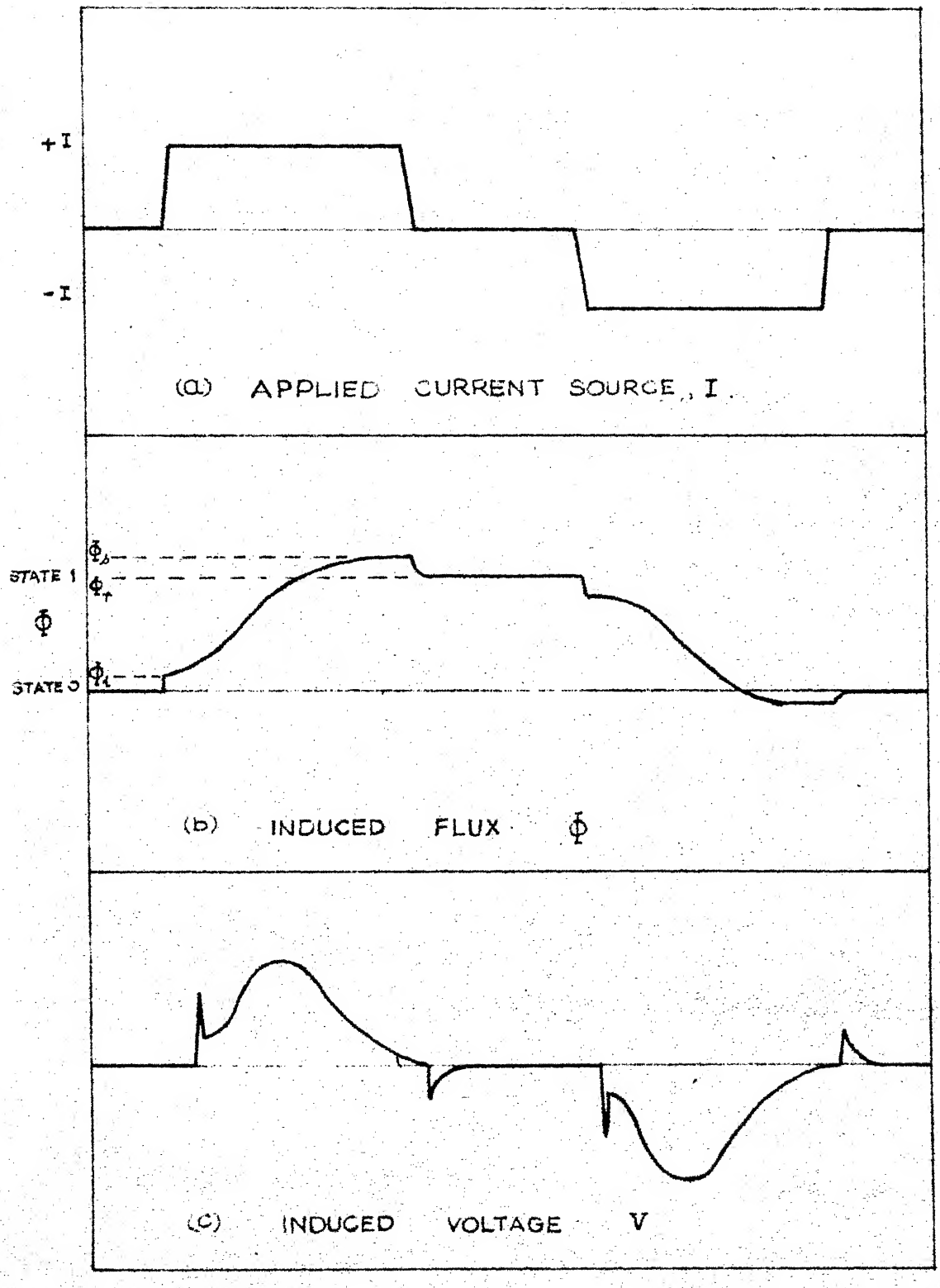
The electrons in every atom of material spin on their own axis forming small current loops with associated magnetic flux vectors. In ferrite materials a group of neighbouring atoms with net electron spin all contributing to a flux B in the same direction tend to act as a single entity called a magnetic domain. Within each domain all the electron spins are parallel to each other. Adjacent domains have different directions of spin. The region between two domains is called the domain wall. Here the spin directions gradually change as the wall is crossed from one domain to another. In unmagnetised material the domain may have a linear dimension of

0.1 mm.; the wall thickness is about 10^{-4}mm.

When an H field is applied to the material, the domains reorient themselves such that the net B in the direction of H increases. Two processes usually take place in this orientation. Domain walls move and domains combine into larger ones with net B in the direction of H. This is called domain wall motion. Domains may also rotate to align themselves in the direction of H. This reorientation of domains may be reversible or irreversible. In the reversible case the domains return to the original orientation when the H field is removed. In the irreversible case the domains remain in the reoriented direction after the H field is removed Irreversible change takes place if the applied field exceeds the coercive field H_M of the material.

The B-H loop gives only the static characteristics of the core. When a step change of H is applied so that the material is in the reversible region, domains reorient themselves mostly by rotation. This is a rapid process and takes typically several nanoseconds to 0.1 microseconds. Irreversible domain orientation takes place mostly by domain wall growth. This is a relatively slow process and typical switching times are of the order of a fraction of a microseond to several microseconds.

Fig. 2.2 illustrates the resulting flux and voltage variations when a core is switched by a constant current source. There is an initial rise in the flux, ϕ_i, and a


+I
-I
(a) APPLIED CURRENT SOURCE, I.
STATE 1
Φ
STATE 0
(b) INDUCED FLUX Φ
(c) INDUCED VOLTAGE V

peak in the voltage induced associated with the initiation of the current from the source. As the domains become aligned, the flux increases with its rate of change being reflected in the magnitude of the induced voltage. This induced voltage appears as a counter e.m.f. in the primary and as an induced e.m.f. in the secondary. When the saturation flux, ϕ_s, is reached there is no further increase in the flux and the voltage drops to zero. When the current is turned off, the flux is slightly reduced to the remanent value ϕ_r and a corresponding spike is produced in the voltage. If the current source now reverses direction the core flips back to its original state.

2.3 Switching Speeds :

Over a limited range of applied fields the switching time of a core and its field are related by the formula

$$T (H - H_0) = S$$

where H_0 is a field approximately equal to the coercive force and S is the switching coefficient of the material. Fig. 2.3 shows 1/T plotted against H. There are many ways of defining switching time but the most useful is the period between the time when the drive pulse reaches 10% of its maximum amplitude to the time when the output e.m.f. of the core has fallen to 10% of its peak value. This is shown in Fig. 2.4. The definition assumes that the rise time of the drive pulse is considerably faster than the time taken for the output to reach its

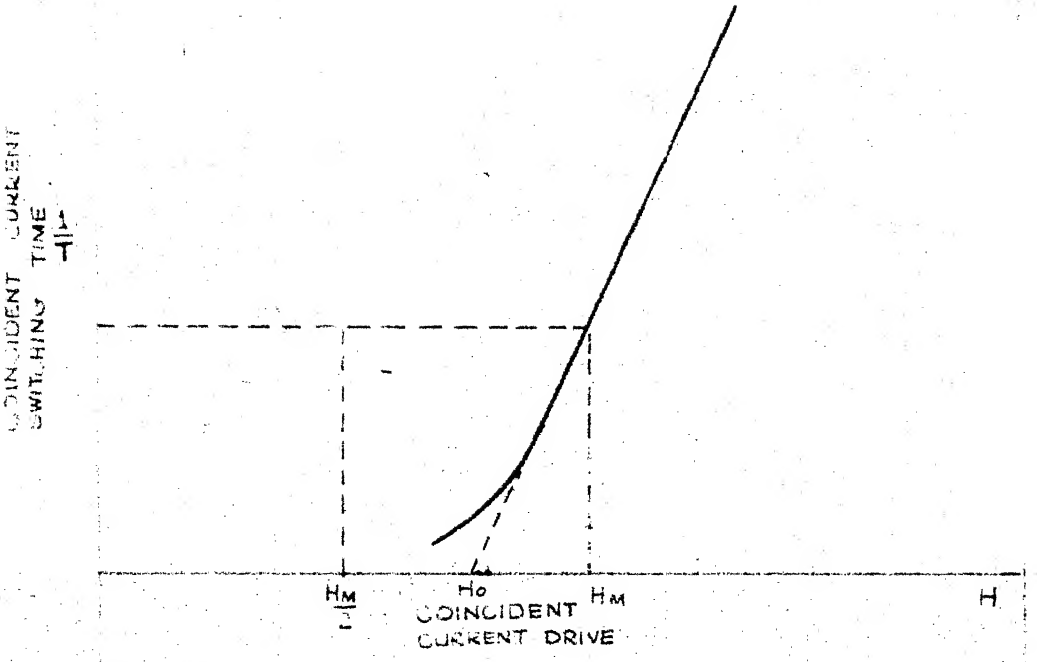


FIG. 2·3

RELATIONSHIP BETWEEN SWITCHING TIME AND APPLIED FIELD

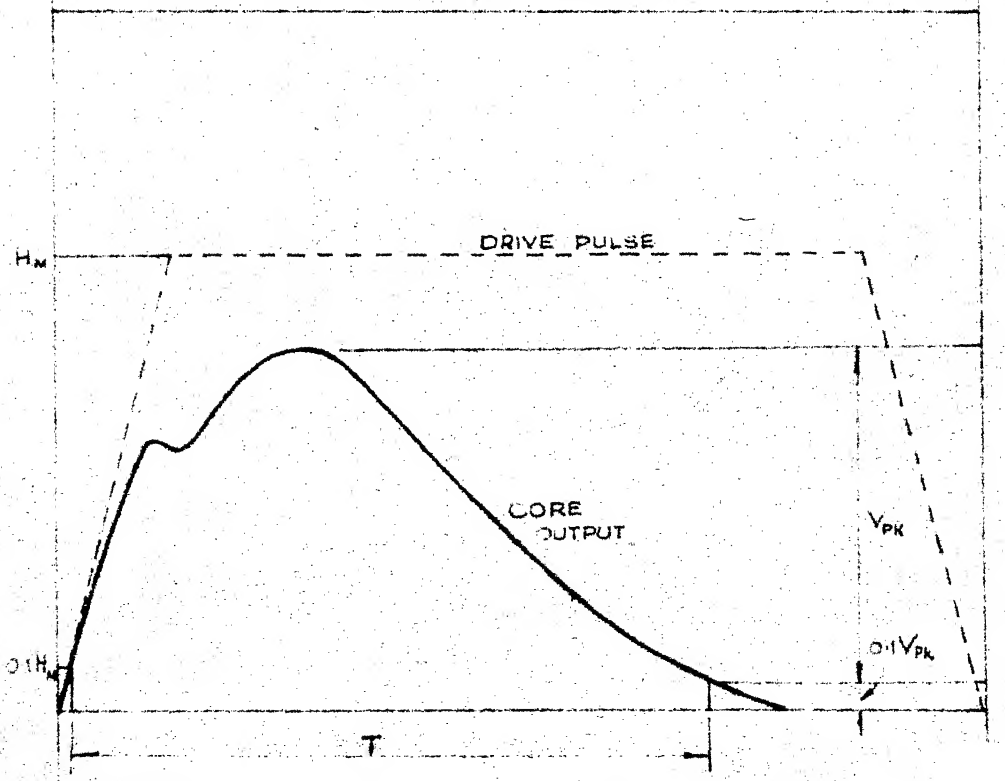


FIG 2·4

peak value, otherwise the switching time will be increased.

Owing to the common use of coincidence systems the switching times are often quoted without specifying the drive currents. In this case, a driving field H_M of about 1.3 H_C is assumed as this is the optimum field to yield the maximum squareness ratio.

The switching coefficients of available materials lie approximately in the range 0.7 to 0.8 microsecond oersteads. H_0 ranges from 0.6 to 3 oersteds. Since the ratio of H_M to H_0 is fixed in a coincident drive system it is obvious that a core with a higher H_0 will switch more rapidly, though it will require a larger drive to do so. The nature of the plot of coincident current switching times against coercive force is given in Fig. 2.5. It has been shown that the formula $T (H - H_0) = S$ holds upto a value of applied field from two to five times the coercive force. Above this point S falls to a value of about 0.3 microsecond oersteds and even lower at higher drives. These variations in S have been explained by assuming that the mode of switching changes as the drive increases, the first fall being attributed to a change from the domain wall movement to domain rotation and the second by a change over to coherent rotation of the total magnetisation within the torroid. However, this condition of a large drive does not arise in a coincident current store where the maximum drive is limited.

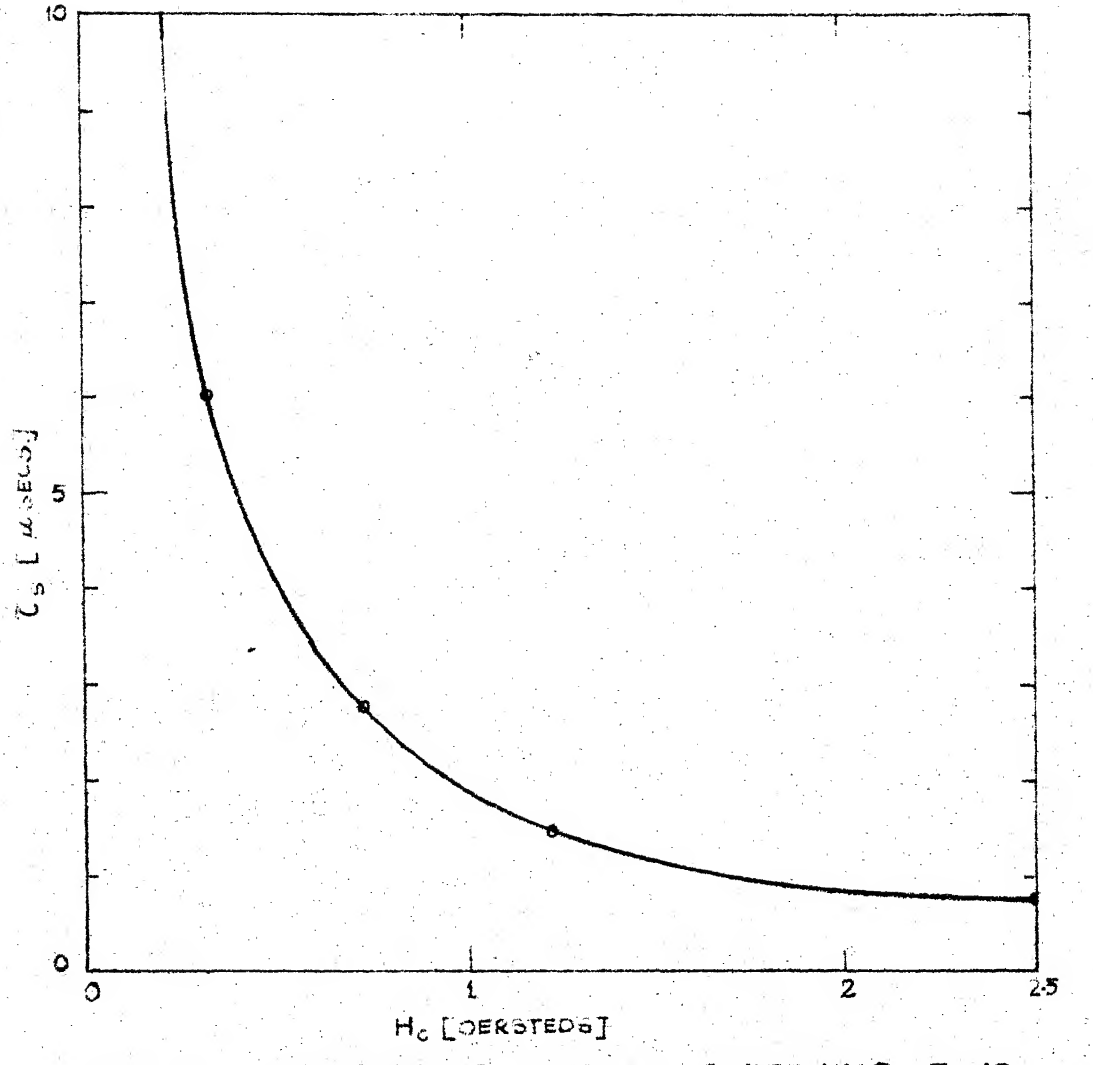
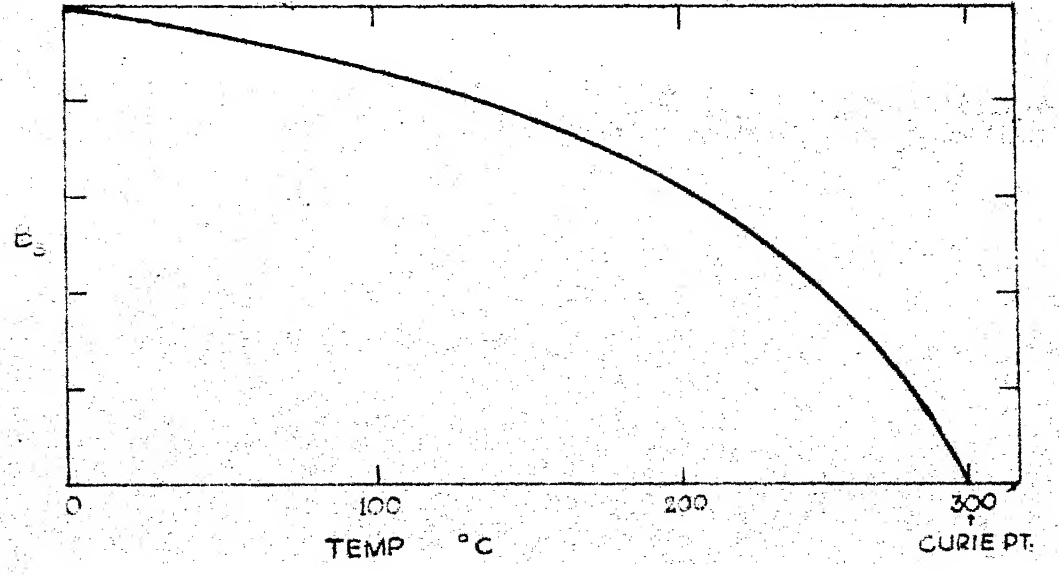


FIG 2-5 COINCIDENT CURRENT SWITCHING TIME AND H_c FOR TYPICAL FERRITES



2.4 Temperature Effects :

For most square loop ferrites the Curie point lies in the region 150°C to 300°C. As the temperature of the core increases both the saturation flux B_S and the coercive force H_C decrease, finally reaching zero at the Curie point. Temperature rise may be attributed to change in ambient temperature and self heating due to switching losses in the core. A 10° to 20°C rise is often sufficient to impair the discrimination in a large store owing to the consequent reduction in coercive force which increases the f lux change in cores subjected to half drive pulses. Any further increase might cause irreversible flux changes under the action of these pulses so that serious loss of information would result. The best solution to this problem is to use a thermostatically controlled enclosure for the matrix. However, this is no solution in faster coincident drive stores when the same address is allowed to be repeatedly selected at the maximum repetition rate. In this case, the temperature rise may be minimised by using the smallest available cores which will provide the most favourable ratio of volume to surface area and the shortest distance for the heat to travel from the interior of the core to its surface. The nature of variation of flux density with temperature for a typical core is shown in Fig. 2.6.

2.5 Core Testing :

Since 100% reliability is required, it is necessary

to test each core before it is used in the stack. Two types of testing procedure are applied to the cores. The first of these, a low frequency loop test, measures the parameters of the saturation loop. The second is used to determine their suitability for incorporation in a store using coincident current selection.

The low frequency loop test :

The main requirements for this test are that the ratio of permeability at saturation, μ_c , to the permeability as B passes through zero, μ_s , be as small as possible. These parameters may be determined by applying to the core, a sinusoidal current, I, of sufficient amplitude to take the core well into saturation in both directions. Fig. 2.7 shows the circuit used to obtain the core output which may then be used as follows:

(a) μ_c is derived directly from the peak value of the core output e.m.f.

(b) H_C is determined by measuring I when the core output e.m.f. reaches its peak.

(c) μ_s follows from the value of the core output e.m.f. when I passes through zero.

No rigorous determination of the parameters was done from this test. It was performed to obtain a rough value of H_C and hence determine the value of current required to switch the core between remanent states.

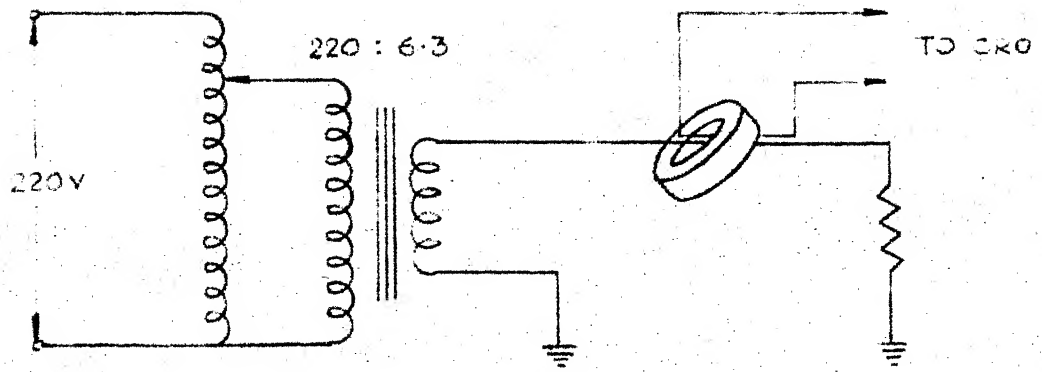


FIG 2·7 CIRCUIT FOR LOW FREQUENCY LOOP TEST

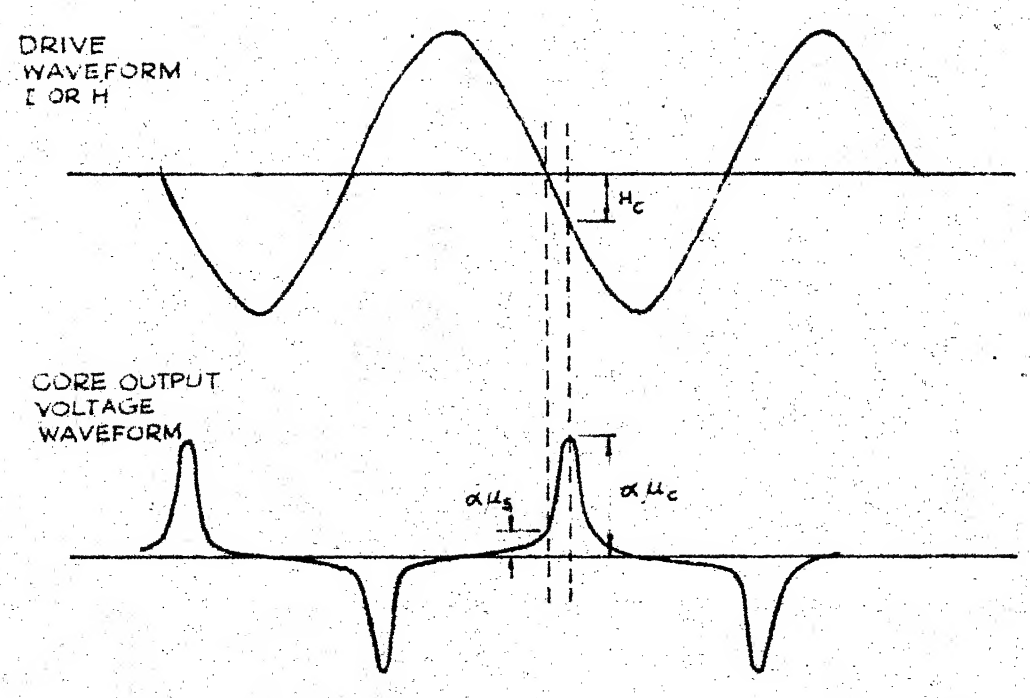


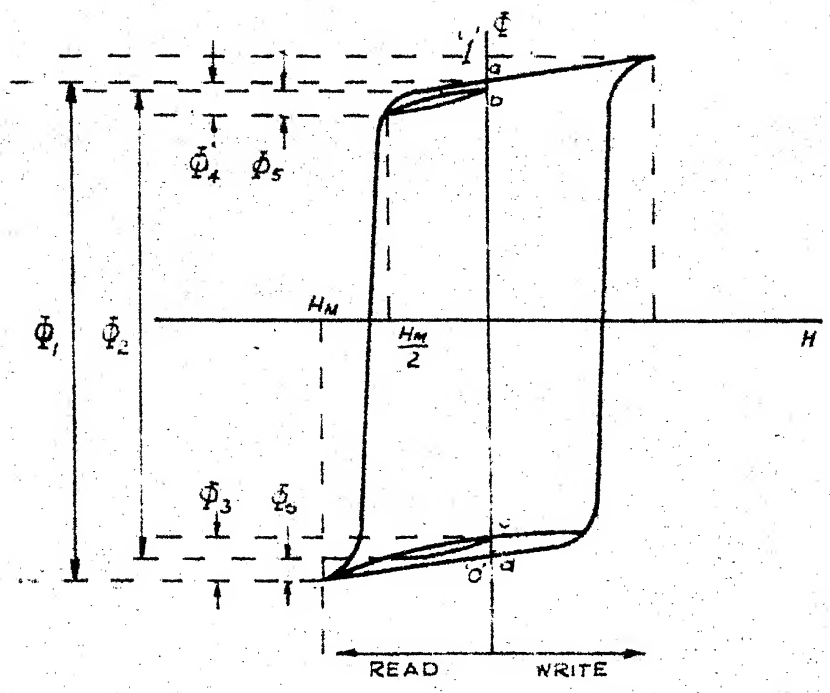
FIG 2·8 LOW FREQUENCY LOOP TEST

The pulse test :

The low frequency loop test does not provide enough information about the core to make it possible to assess its value as a storage element in a coincident drive matrix store. In the pulse test, the core is tested with pulses that are likely to be encountered during operation in a coincident drive matrix store.

Referring to Fig. 2.9, when core is in the upper remanent state, it is assumed to be storing a logical '1' and when in the lower remanent state, a logical '0'. In order to determine the state of the core, a full current pulse is applied in the negative direction. All outputs likely to arise in a coincident current store are given in Table I which refers to Fig. 2.9.

The first half read pulse after a logical '1' has been written produces irreversible change of flux from a to b and hence the output from this pulse is somewhat larger in amplitude and longer than those from subsequent half pulses in the same direction which produce only reversible changes. Read pulses will not normally be applied to a core in the lower remanent state d, since in a computer a read process is normally followed by a write process in which a core experiences at least a half write pulse which would return it to point c. Thus the logical '0' outputs are assumed to arise from a core at c and not d. The first three outputs in Table I are due to full pulses acting on the selected core. The



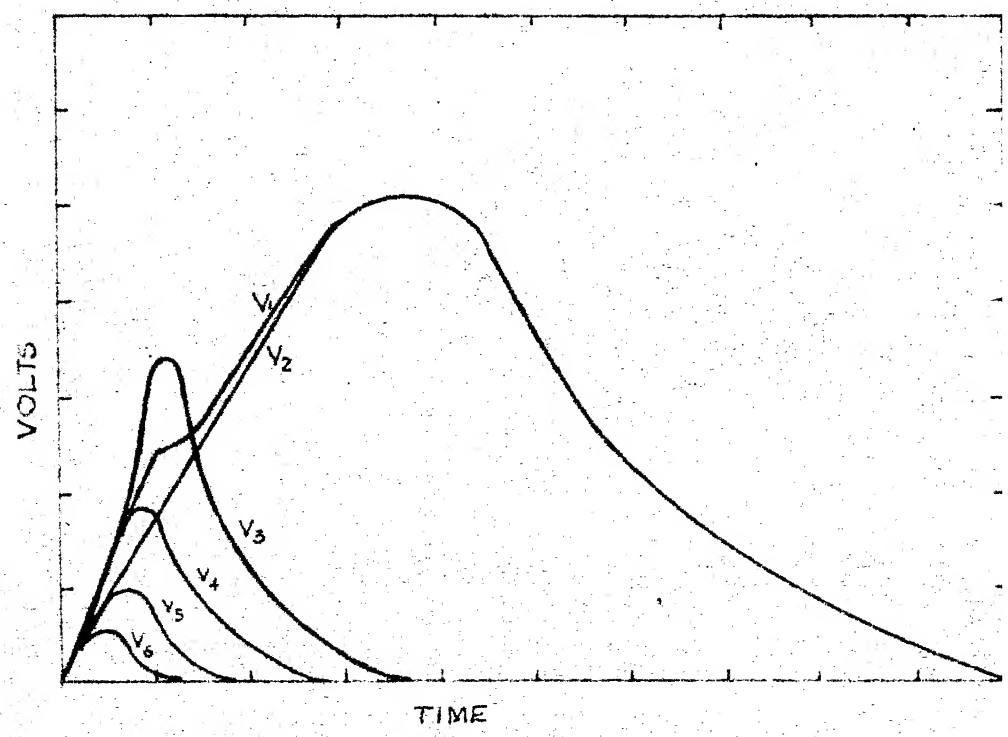


FIG 2·9 FLUX CHANGES AND OUTPUTS IN CCM

OUTPUT	SYMBOL	DRIVE	INFORMATION STORED	FLUX CHANGE	OUTPUT VOLTAGE
UNDISTURBED '1'	uV_1	H_m	'1'	Φ_1	V_1
DISTURBED '1'	τV_1	H_m	'1'	Φ_2	V_2
DISTURBED '0'	dV_2	H_m	'0'	Φ_3	V_3
FIRST DISTURBED '1'		$H_m/2$	'1'	Φ_4	V_4
'1' DISTURB	τV_{n_1}	$H_m/2$	'1'	Φ_5	V_5
'0' DISTURB	τV_{n_2}	$H_m/2$	'0'	Φ_6	V_6

TABLE - I

remainder arise from any other core which receives a half pulse and since one problem in a store is to distinguish between a '1' and a '0' output in the presence of many disturb outputs, it is evident that V_1 and V_2 should be as large as possible compared with the others.

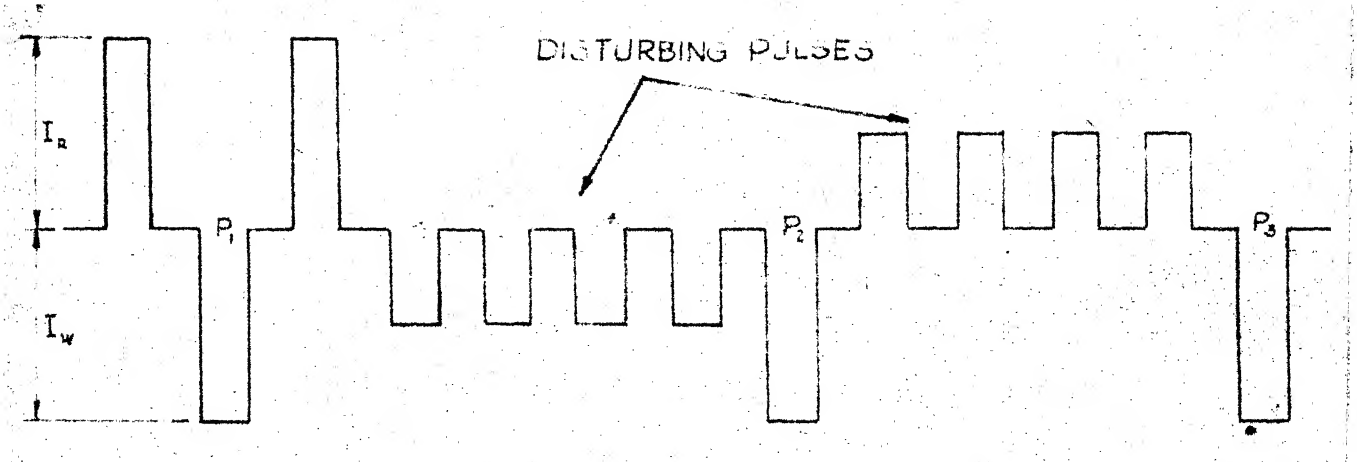
The pulse train shown in Fig. 2.10 was used to test the cores. These pulses are generated by the circuit whose block diagram is given in Fig. 2.11. Fairchild Micrologic Integrated circuits were used to fabricate the entire circuit. The configuration of the current drivers is similar to those discussed in Chapter V.

Results :

The results of the Low frequency loop test showed that a current of 500 milliamperes was sufficient to switch the cores between remanent states.

On the basis of these results the half read current was selected as 400 milliamperes for the pulse test. A typical set of outputs is given below :

Undisturbed '1' output	80 millivolts
Disturbed '1' output	75 millivolts
Undisturbed '0' output	11 millivolts
Disturbed '0' output	9 millivolts
Switching time	1.6 microseconds
'1' peaking time	0.8 microseconds



P_1 GENERATES uV_1

P_2 GENERATES tV_1

P_3 GENERATES dV_2

FIG 2·10 PULSE TRAIN FOR CORE TESTING.

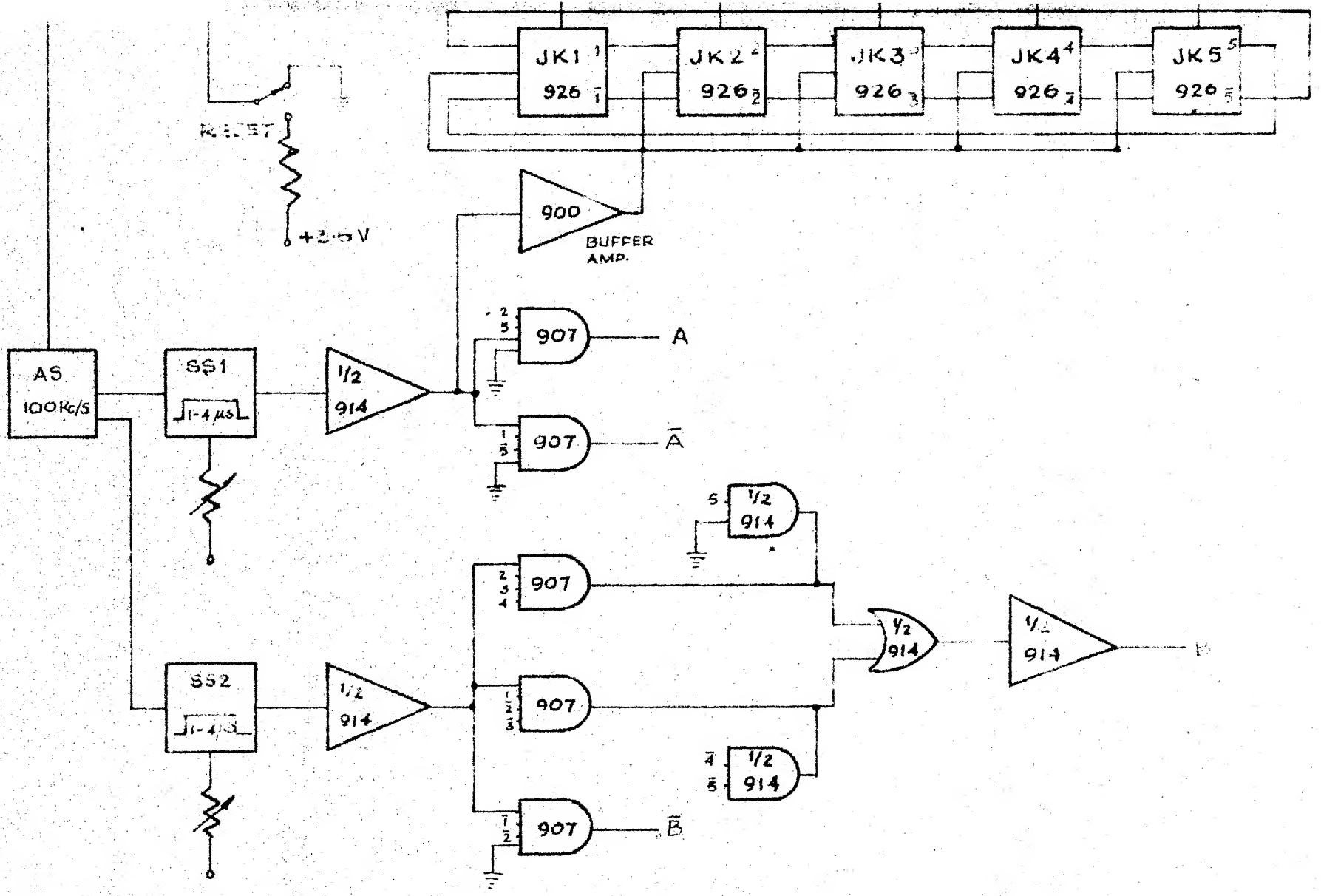
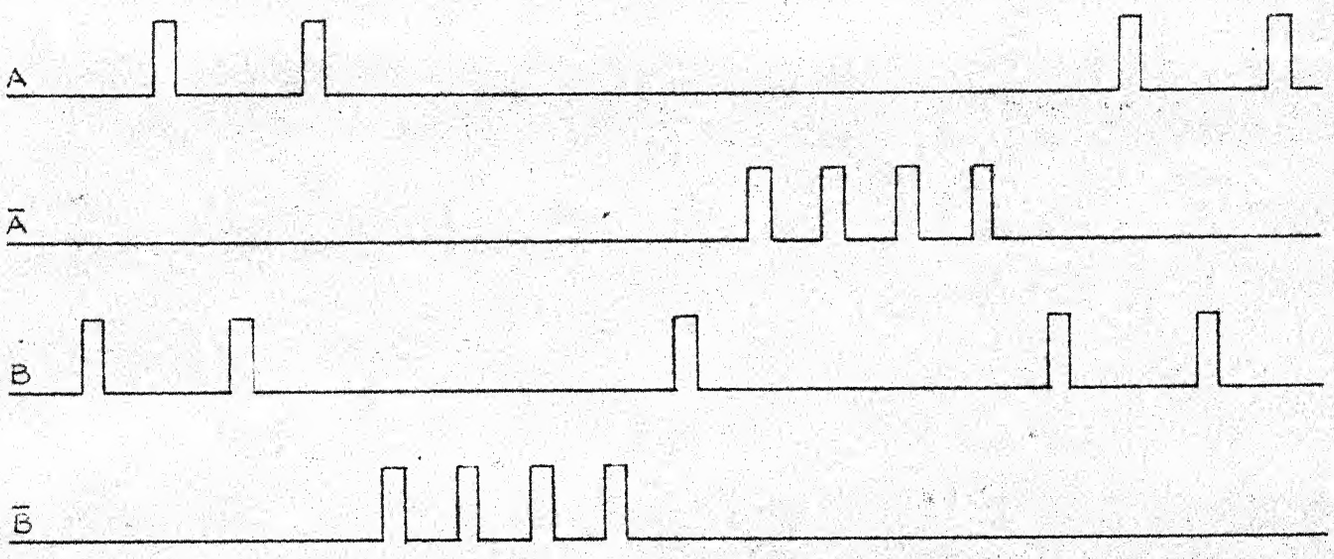


FIG 2·11A BLOCK DIAGRAM OF WAVEFORM GENERATOR FOR PULSE TEST



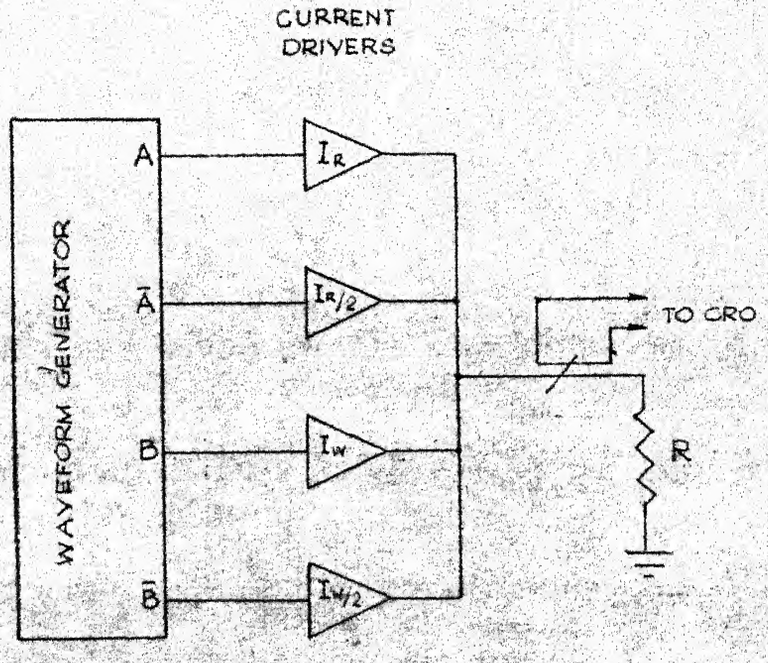


FIG 2-11B PULSE TEST

CHAPTER III

BASIC MEMORY CONFIGURATIONS

There are two major types of random access magnetic memory, the coincident current memory (CCM) and the linear selection memory (LSM). These memories are used to store words of information. A word is a block of binary data of a given number of bits. The number of bits is determined by the parent data processing system. Each word is stored in a given address which is a spatial location in the memory. The address is determined by the state of an address register at the time of inserting the word. A set of magnetic cores constitutes each address, one core for each bit of stored word.

The typical ferrite core memory, whether CCM or LSM, is composed of a number of memory cores arrayed in a set of parallel planes forming a three dimensional matrix, surrounded by associated driving and sensing circuitry. The memory cores of the matrix are arranged in a set of planes in the X Y dimension, called bit planes. The cores representing a given word are arranged in the Z direction, one per bit plane in the same relative position in each plane. Each line of cores in the X direction is called a row and in the Y direction, a column.

3.1 Memory Wiring :

The wiring in a memory matrix provides circuits for core driving currents during both read and write and for sensing outputs during read. A great variety of wiring patterns are used; some LSM systems require just two windings per core, but most CCM and LSM systems require three to six wires. The

wire serves as a physical support for the cores and in addition must be arrayed in such a way as to cancel or at least minimise, inductive coupling between adjacent windings. In some CCM and LSM systems, bidirectional windings are used to perform the read/write function; in others, separate unidirectional windings are used, doubling the winding requirement, but simplifying current driver design.

In addition to the drive windings which pass through all bit planes, two other windings which pass through all the cores in a single bit plane are required. One of these windings carries pulses which control the inserting of 'ONES' and 'ZEROS' and the other carries the induced voltage output of the selected core. These two windings may be combined into a single winding since one is required during writing and the other during reading. However, individual windings are more often used to eliminate the need for short delays between operations and to reduce noise in the sensing operation. Thus the most satisfactory wiring scheme consists of four wires threading each core - two for X and Y read/write and one each for inhibit and sensing operations, as shown in Fig. 3.1.

3.2 Memory Operation :

Each memory core stores a binary 'ONE' or 'ZERO'. Any pair of remanent flux states that can be read so as to induce output voltages which are clearly and consistently distinguishable from each other can be used to represent 'ONES' and 'ZEROS'. In the design of ferrite core memories, it is

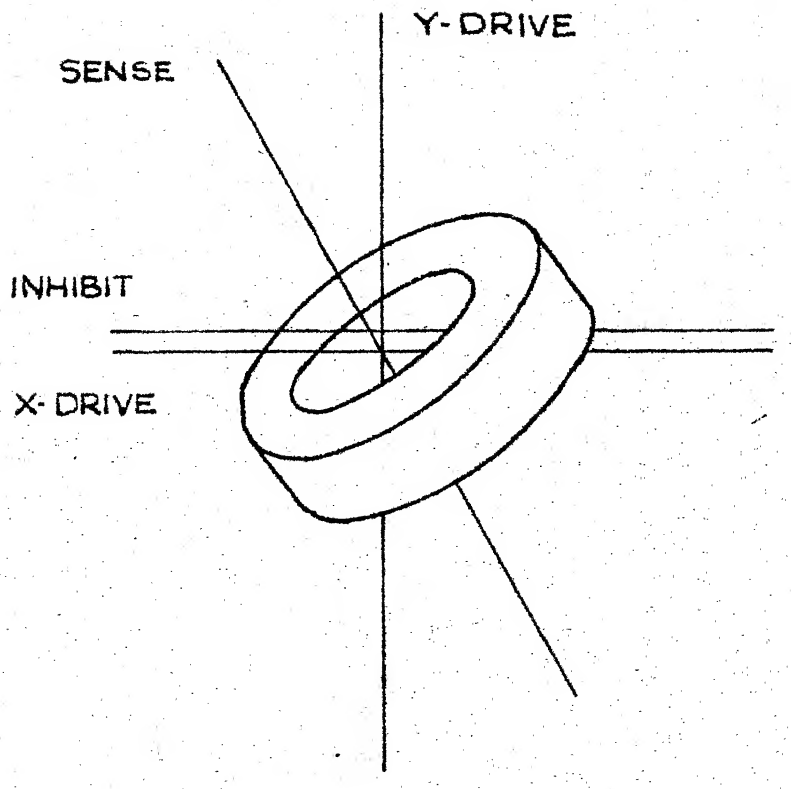


FIG 3·1 TYPICAL WIRING ARRANGEMENT FOR A COINCIDENT CURRENT MEMORY

generally necessary to operate on one of a family of roughly symmetrical hysteresis loops in which flux changes are somewhat less than those produced by alternate applications of saturating m.m.f. These loops generally exhibit a higher squareness ratio than the major loop and are more adaptable to operations requiring partial core selection.

The function of a full select current is to drive the memory core flux in the 'ZERO' direction or in the 'ONE' direction. When the core is in the 'ONE' state, a current of the proper amplitude, duration and polarity will switch the core to the 'ZERO' state, inducing a voltage in the sense winding.

Since ferrite cores switch between states in a nearly square hysteresis loop, the effect of noise is usually small and the discrimination of 'ONES' and 'ZEROS' in the induced voltage output is good. Proper design of the sense amplifiers provides a consistent 'ONE' to 'ZERO' discrimination.

Read out is destructive and the word read must be stored momentarily in the memory register for subsequent writing. A word in this register is also available as output. A new word may be substituted optionally into the memory register prior to the write operation. Since all the selected cores are in the 'ZERO' state after read, the writing operation consists of entering 'ONES' in appropriate cores and leaving the remaining cores in the 'ZERO' state. A write pulse tends to write 'ONES' in all cores of that location, whereas information pulses designated by the memory register are applied

individually to each bit plane to control the write operation so that those cores which are to store a 'ZERO' do not switch to 'ONE', but the others do. In CCM, writing is done by triple coincidence, and in LSM by double coincidence. Unselected cores in both CCM and LSM are disturbed during write, but to a greater degree in CCM.

3.3 CCM Form and Operation :

In a coincident current memory all cores in a selected address are switched by the coincident action of a pair of currents.

The memory cores in a typical CCM are arrayed in a set of bit planes, each plane including one bit of all words. A sense amplifier and an inhibit driver are associated with each bit plane. Each row or column drive winding links all cores in one row or column of all bit planes. A sense winding and and inhibit winding each link all cores in one bit plane, the sense winding functioning during read and the inhibit winding during write. The sense winding is in most cases bipolar. The geometry of the winding pattern is such that half of the cores in the plane are sensed in one direction and half in the other direction. Thus, in effect, noise output of any pair of distrubed cores are mutually cancelled. The cumulative noise effect in the bit plane is thus greatly reduced.

When a word is to be read from or written into the memory, the set of memory cores storing the word is driven by full read currents. When the parent system determines that a

word is to be read, a coded address is transmitted to the memory to initiate the read/write cycle. One row selection circuit and one column selection circuit are energised to route the half read pulses into one row and one column. The combined full read current at the row/column intersection drives the cores in the 'ZERO' direction. Sense amplifiers discriminate between 'ONES' and 'ZEROS' in the induced output in each bit plane. The read word is replaced in the memory by causing the appropriate row and column selection elements to route the half write currents into the same row and column lines. The combined full write current drives the selected cores in the 'ONE' direction and the presence or absence of the inhibit pulse under memory register control, controls the writing of a 'ZERO' or 'ONE'.

A typical CCM array is depicted in Fig. 3.2

3.4 LSM Form and Operation :

The coincidence storage system places rather stringent requirements on the squareness of the cores and on the drive pulses in order that information should not be partially erased or inserted by the half current pulses used for reading and writing. These problems are more or less overcome in the LSM organisation.

Cores are arranged in a matrix as shown in Fig. 3.3. Each word location has its own read drive wire, so that a drive pulse is applied only to the cores in the selected word. A word is read by sending a full read pulse through the decoded

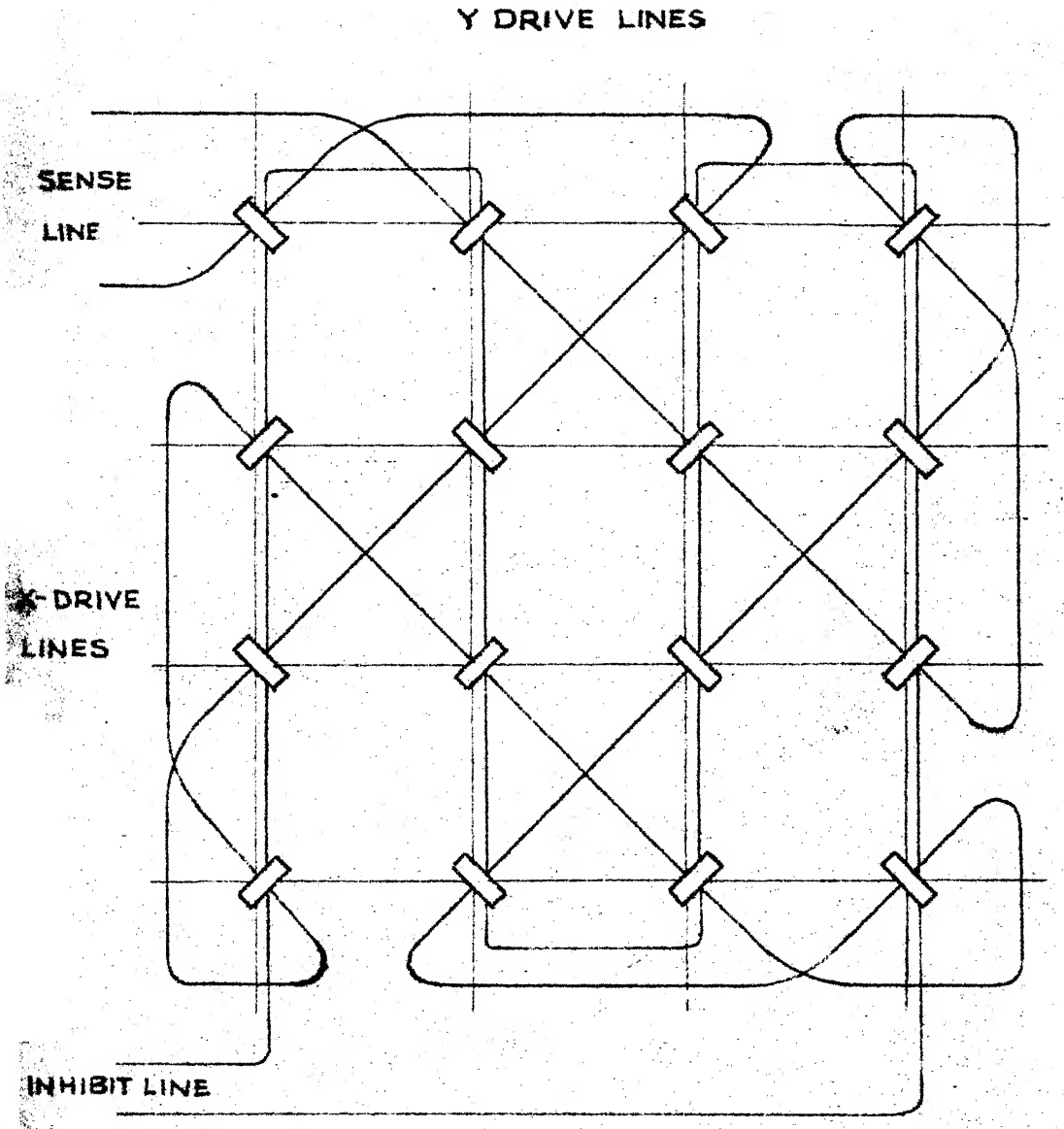


FIG 3-2 CCM ARRAY 16 WORDS

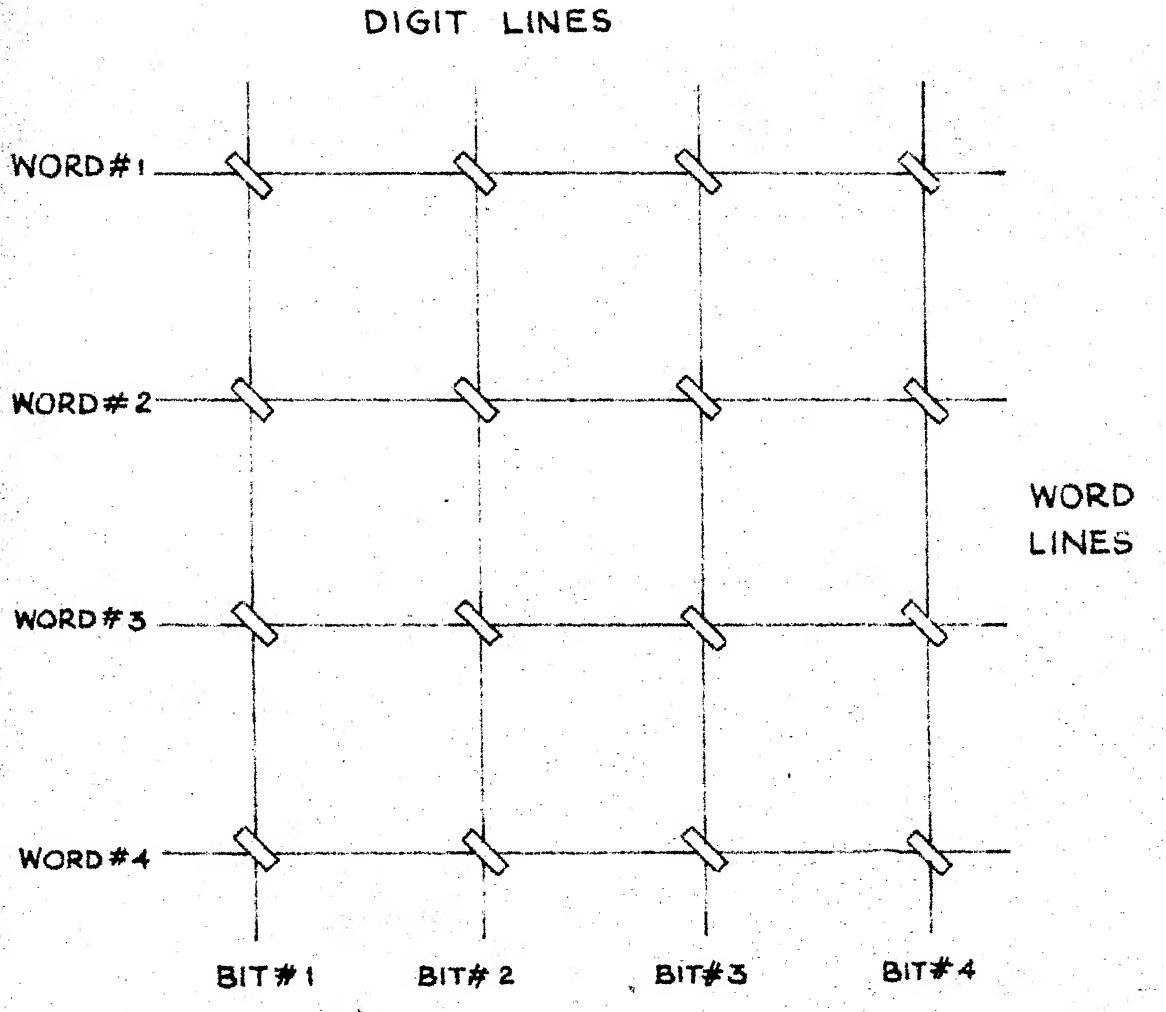


FIG 3·3 LSM ARRAY, 4 WORDS, 4 BITS PER WORD

word line. The fact that the read line threads only the cores of the selected word means that there is no limit on the amplitude of the read pulse and by using a larger drive than can be applied in a CCM, a larger amplitude 'ONE' output is obtained. In addition a faster output is also obtained which leads to a shorter access time.

After reading, all the cores in the selected word are left in the 'ZERO' state. Unlike the reading process, writing cannot be performed by applying the same full drive pulse in the opposite direction since some cores are required to store a 'ZERO'. This process is done by a coincidence technique. One component pulse is carried by the word line and the other by the digit wire which threads cores in the same position in each word. The digit pulse, the presence or absence of which determines the information stored, may take the form of an inhibiting or augmenting pulse.

In the augment system a half write pulse on the word line is added to a half pulse on the digit line when a 'ONE' is to be written. A core into which a 'ZERO' is to be written receives no digit pulse. Disturbing pulses are all in the write direction and hence can affect only a stored 'ZERO'.

In the inhibit system a full write pulse is carried by the word line of the selected word. This is opposed by a half pulse on the digit wire when a 'ZERO' is to be written. In this case the disturb pulses which could cause trouble are the single half pulse in the write direction when a 'ZERO' is

written which might lead to a larger 'ZERO' output and the digit pulses in the read direction for other addresses which might tend to destroy a stored 'ONE'.

In both systems, therefore, a core storing a 'ZERO' receives one disturbing pulse in the write direction from the word line during the writing process but stored 'ZEROS' are affected by the digit pulse in the augment system and stored 'ONES' are affected in the inhibit system.

All the advantages of the LSM operation are offset by the increased cost of the selection circuits as compared to a CCM of the same size. In addition they are more difficult to design satisfactorily. The fact that LSM has not been much used suggests that it is not an attractive proposition for a large store.

A careful comparison between CCM and LSM seems to suggest that CCM is the better system. Even though LSM can undoubtedly achieve higher speeds, the speed attainable by CCM is fast enough for present day commercial computers where its relative cheapness is of more importance.

CHAPTER IV

THE BASIC BLOCK DIAGRAM OF A CCM SYSTEM

4.1 The General Layout :

The block diagram of Fig. 4.1 shows the general arrangements of the major circuits essential for the operation of a typical random access coincident current store.

The matrix stack consists of W planes each of dimension N x N. Each of the X and Y drive lines is driven from the X and Y line selection drivers. These circuits are responsible for routing the read and write current pulses from the drive current generators into the selected X and Y lines. Only one line selection driver on each of the X and Y lines is selected by the decoders. Thus the READ/WRITE pulses are routed into one X line and one Y line only. Inputs to the N output decoders are obtained from the Memory Address Register, MAR. As the name implies, this register stores the address of the location from where information is to be retrieved or inserted. The Memory Buffer Register, MBR, contains the information which is to be inserted or which has just been retrieved. The outputs of the MBR are connected to a set of Inhibit drivers. These circuits control the storing of information into the memory. The Central Processing Unit, CPU, communicates directly with the MBR for all input and output operations from the memory. The Timing Generator generates the various pulses for a single memory read or write cycle on receipt of an initiate pulse from the Central Processor.

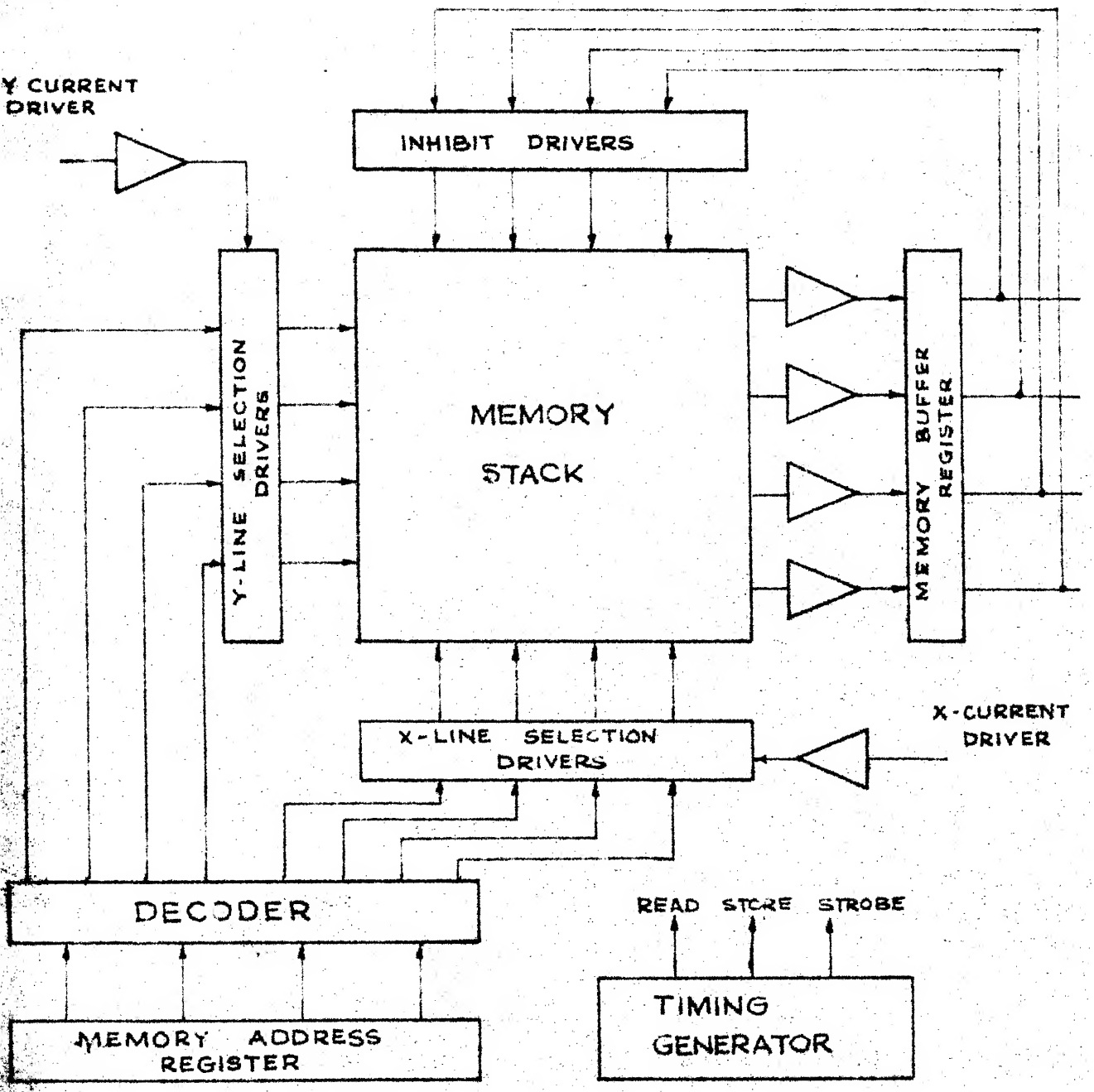


FIG 4·1 BASIC BLOCK DIAGRAM OF A CCM SYSTEM

4.2 Circuit Requirements for a CCM System :

A memory matrix consisting of W planes each of size N x N, when used in a coincident drive system, can store N^2 words each of length W bits. The word length is dependant on, firstly, the number of words that can be stored in the stack, secondly, on the number of instructions the CPU uses, and thirdly on the provisions for indirect addressing. In some memory systems where the memory is divided into sectors, the word length will also depend on the number of such sectors. In order to optimise on the number of circuits, N is chosen to be an integer power of 2.

For a memory storing N^2 words, and attached to a CPU using P opcodes with no provision for indirect addressing, the word length W is given by : $W = p + n$ where p and n are such that $2^n = N^2$ and $2^p = P$. Thus any instruction word consists of the opcode of length p and the address part of length n. Since each X line and each Y line is associated with a line selection driver, 2N such circuits are required. Two READ/WRITE current drivers are required, one for the X lines and one for the Y lines. The N output decoders are fed from I inputs such that $2^I = N$. Consequently the MAR consists of 2I flip flops - I for the X lines and I for the Y lines. The size of the MBR is determined by the word length. It will thus consist of W flip flops. This further fixes the number of Inhibit drivers to W.

As an example consider a 256 word memory attached to a

CPU utilising 16 opcodes. The memory has internal parity checking.

Since $N^2 = 256$, $N = 16$

Number of line selection drivers $= 2N = 32$

The decoders have 16 outputs

Number of inputs to the decoders is such that $2^I = 16$

Therefore $I = 4$

Thus the MAR requires 8 flip flops

Length of the opcode part of the word is such that

$$2^p = P = 16$$

Therefore $p = 4$

Length of the address part of the word is such that $2^n = N^2 = 256$

Therefore $n = 8$

One additional bit is required as the parity check bit

The word length is therefore $4 + 8 + 1 = 13$ bits

Number of Inhibit drivers = 13, and the MBR requires 13 flip flops. This completes the detailed requirements for a 256 word coincident current memory.

CHAPTER V

MEMORY PERIPHERAL CIRCUITS

The memory peripheral circuits which must be regarded as part of the store account for a large fraction of the total cost and are also the most likely source of unreliability. Since the possible organizations of the storage elements themselves are limited, the success of the store depends mainly on the efficient design of the input/output circuits. These circuits are discussed in some detail in this chapter.

5.1 The MAR and MBR :

A register is a unit which stores information temporarily during processing. In the course of a single operation, several numbers may be manipulated and it is necessary to hold these data while they are operated upon.

Basically, a register is nothing more than a set of flip flops. If the flip flops are connected in series, they form a serial bit register. A word is inserted into such a register at one end, one bit at a time. In a parallel bit register each flip flop has independent input lines. Information is entered into and retrieved from such a register a word at a time. This results in much faster operation, but requires more circuitry.

In the 256 word memory the MAR is an eight bit parallel register. It stores the address of the memory location from where information is to be retrieved or into which information is to be inserted. The MBR is a thirteen bit parallel

register. At the end of a read operation it contains the word located at the address specified by the MAR. At the beginning of a write operation the MBR contains the word that is to be written into the location whose address is contained in the MAR.

The flip flops are of the conventional set-reset type and consequently further details regarding their design will not be discussed.

5.2 Sense Amplifiers :

The sense amplifiers for a randomaccess core memory require the main design emphasis. When data is taken from a coincident current ferrite core memory, it comes out as electrical pulses on a group of wires. One such wire is required for each bit in the word. Thus, in a parallel access matrix store, the number of output amplifiers is determined by the word length since one amplifier is needed for each digit position.

The sense winding links all cores storing the same significant bit of every address. Information signals result from flux excursions of the memory cores from $-\phi_r$ to $+\phi_r$, caused by application of read currents. Ordinarily the presence of a pulse indicates a 'ONE' bit and the absence of a pulse at the proper time indicates a 'ZERO' bit. The sense amplifier accepts these pulses, rejects noise pulses, shapes the signal, amplifies it, and drives logic circuits through which data is transferred to the computers central processing unit.

The design of the sense amplifiers is further complicated by the fact that noise voltages exist on the sense winding at times other than read time. The two types of noise that appear on the sense winding are common mode noise and differential noise.

Common mode noise is the noise voltage that occurs with the same polarity at both ends of the sense wire. It is caused by the inductive coupling from the relatively large currents that write information into the memory cores, across the closely spaced wires on which the cores are strung. Differential noise arises from fully selected cores that do not switch because they are already in the 'ZERO' state and from half selected cores. By winding the sense wire in a cancelling manner this differential noise can be minimised. This introduces a further complication in the design since the amplifier must now be able to amplify bipolar signals to produce unipolar amplified signals on the output.

A sense amplifier must reject differential signals below a fixed threshold value. Thus it must incorporate some form of threshold circuit. The threshold level may be made variable for optimum signal to noise discrimination. The amplifer must be able to reject common mode noise several volts in amplitude, yet be sensitive enough to detect small differential voltages of either polarity. Therefore the input stage normally consists of a differential stage fed by a current source. Determination of whether the voltage read from the

memory represents a 'ZERO' or 'ONE' is accomplished by the decision element in the sensing system. To assure an optimum signal to noise ratio in the signal applied to the decision element, a strobe is employed. This also serves to disable the amplifier and make it insensitive to noise voltages at all times except read time.

Amplifier Requirements :

The most important amplifier requirements are considered to be, input impedance, common mode rejection, frequency response, gain and gain stability, dynamic range, bipolar amplification and rectification, and D.C. restoration and discrimination. Each of these requirements will now be briefly considered.

Input Impedance :

The amplifier input impedance is influenced by four factors; core loading effects, signal waveshape, sensing system frequency response, and characteristic impedance of the sense winding. Reduction of amplifier input impedance results in loading of the memory cores which is undesirable insofar as it represents a loss of drive m.m.f. and affects the tolerance of the drive currents. The input impedance should be high enough so that the L/R time constant of the input circuit does not restrict the overall frequency response of the sensing system. Furthermore the input impedance should not deviate from the characteristic impedance of the sense line so much that reflections and distortion results. Thus the sense line must be

terminated in such a way that the open circuit waveform for a 'ONE' output is preserved.

Common Mode Rejection :

Common mode signals on the sense line can build up to several volts in amplitude. The input circuit of the amplifier must be designed to reject such signals. With this in view, a differential stage fed from a current source is used as the input stage. The rejection ratio is defined as :

$$\text{Rejection ratio} = \frac{\text{Maximum unidirectional signal}}{\text{Minimum bidirectional signal}}$$

This ratio should be as large as possible.

Frequency Response :

Required frequency response of the amplifier may be determined from a consideration of allowed signal delay and distortion in the amplifier. The amplifier delays, attenuates, and spreads the input waveform, the extent of which is a function of the amplifier upper frequency response. Since the amplified core signal is examined only when the signal to noise ratio is maximum, any amplifer delay will manifest itself in the overall memory cycle.

Amplifiers exhibit different frequency responses depending on the spread of characteristics of the transistors. Since the amplifier delay affects the time at which the strobe occurs, the delay must be small in comparison to the strobe width to prevent variations in signal delay in various sense amplifiers from significantly shifting the centre of the strobe

pulse and the output signal peak. If the variation in amplifier delay is large, the effectiveness of the strobe is negated. Fig. 5.1 illustrates the effects of variations in large signal delay.

The difference in frequency between noise voltages on the sense line and the desired signal can sometimes be utilised to enhance signal to noise ratio, by designing the amplifier to have a sharp roll off at high frequencies. However, in fast switching cores the frequency difference is not large enough for this scheme to be practicable. A bandwidth of 1 to 2 mc/s is found to be quite adequate.

Gain and Gain Stability :

The amplifer input signal may be characterised by an amplitude V_s with a possible fluctuation of $V_s (1 \pm m)$. Noise may be characterised by its maximum value V_n. $V_s$min is defined as the minimum amplitude of the signal during the strobe interval. Thus the minimum voltage V_d which allows a stored 'ONE' to be differentiated from a stored 'ZERO' is :

$$V_d = V_s\text{min} - V_n\text{max}$$

$$= V_s (1 - m) - V_n\text{max}$$

V_d is a function of the core, sense line characteristics and amplifier input impedance. Since V_d from the sense winding is very small, the signal must be amplified by an amount G (amplifier gain) so that an ordinary non linear element can distinguish between noise and signal. Although the signal to noise ratio out of the amplifier is the same as that into the

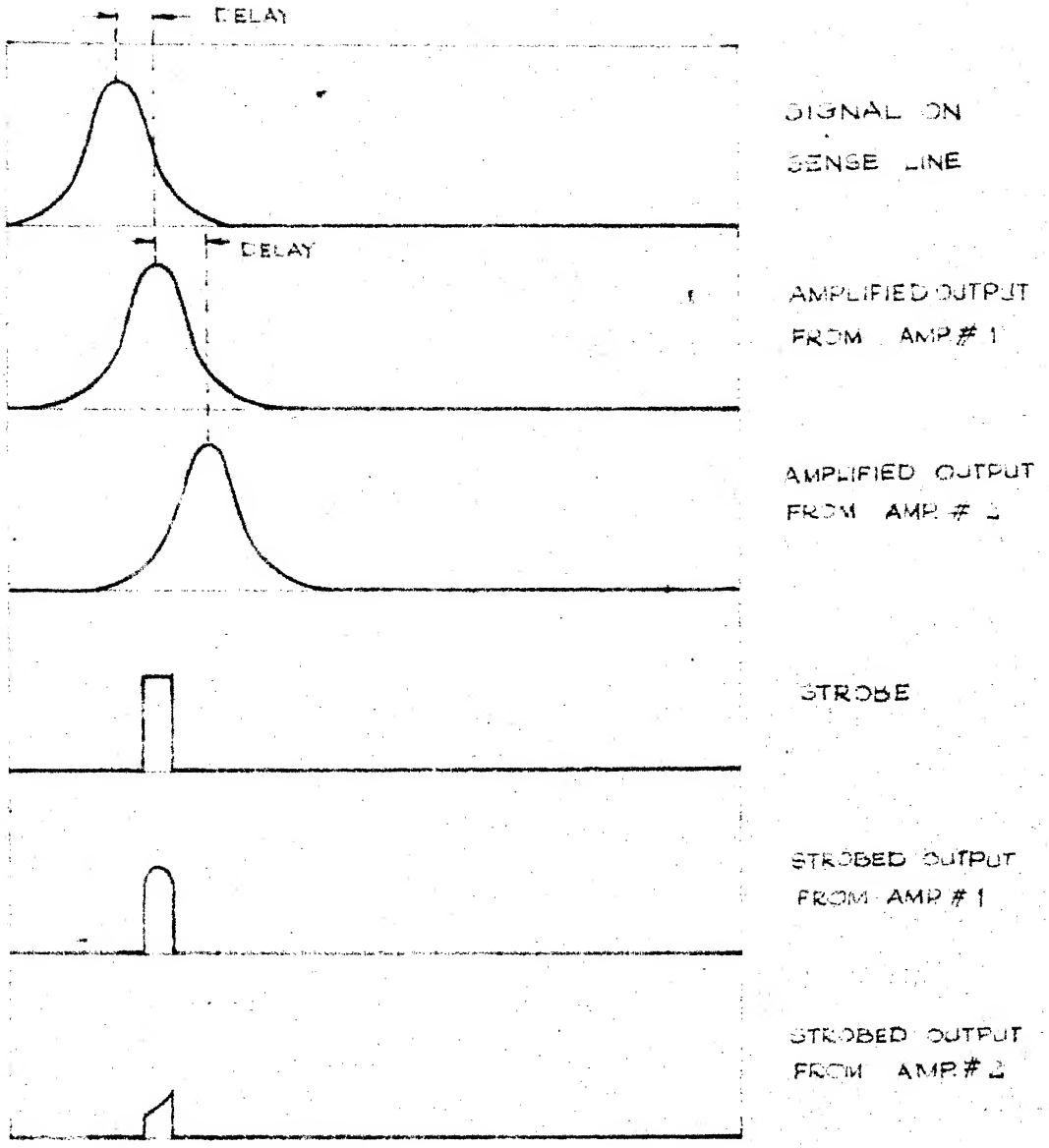


FIG 3-1 EFFECT OF AMPLIFIER DELAY ON STROBING

amplifier, the difference between minimum signal and maximum noise is amplified from V_d to GV_d. If the discrimination circuit is to operate reliably, G should be large and constant for all the sense amplifiers.

Dynamic Range :

The amplifier may be driven by noise voltages much larger than the normal 'ONE' voltage before the desired read signal is applied. It must recover rapidly from this overdrive to adequately amplify the read signal and may be designed to accept worst case noise signals. For a small memory this may be feasible. However, for large memories, where this noise voltage may become several volts in amplitude, such a design may be impractical. Possible solutions to this problem would be to divide the sense winding into small groups or to divide the linear amplifier into two, and insert a limiter.

D.C. Restoration :

Continual changing of information stored in the cores with the same sense winding polarity results in an undesirable D.C. component in the input signal to the sensing system. This component shifts the quiescent output voltage of the sense amplifier and voids the threshold adjustment. This D.C. level shift must be eliminated before the signal is applied to the discrimination system. The problem is serious only in large memory systems. In a small system, the D.C. shift will not be sufficient enough to warrent any special precautions in the design of the sensing system.

Bipolar Amplification and Rectification :

If the sense winding is wound in a cancelling manner signals to be amplified will be bipolar. Since it is inconvenient to design a decision element to operate on bipolar signals, some form of rectification should be introduced before the signal is applied to the decision element. Bipolar amplification increases the dynamic range requirements of the linear amplifier by a factor of two. In large memory systems if the bipolar signals are rectified before being restored, signal distortion is likely to occur. This is due to the fact that rectified positive signals are attenuated and the rectified negative signals are enhanced by the D.C. base line shift. This is not likely to cause any difficulty in a small system where the D.C. base line shift is small.

Description of the Circuit :

The circuit diagram of the sense amplifier which satisfies most of the important requirements is shown in Fig. 5.2.

Transistors Q_1 and Q_2 form a difference pair. The emitters are fed from a constant current source comprising the +6 volt supply and resistances R_3 and R_4. Capacitor C_1 effectively ties the emitters together for A.C. signals. The bases of Q_1 and Q_2 are connected to ground through two 150 ohm resistances which form the terminations for the sense wire. The first stage of the amplifier is directly coupled to the second stage comprising Q_3 and Q_4. In this stage, the bipolar signals

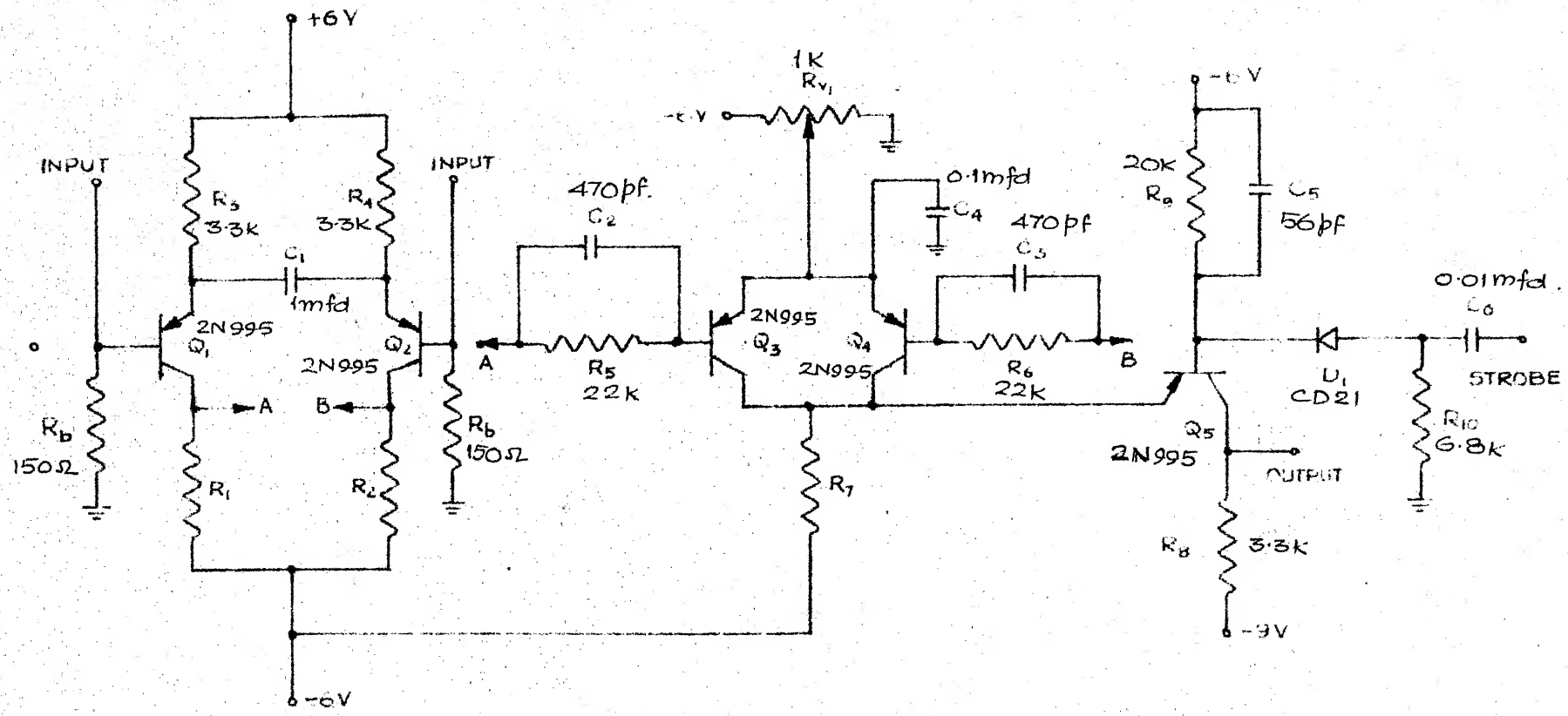


FIG 5·2 SENSE AMPLIFIER

are rectified to produce a unipolar signal at the common collectors Potentiometer RV1 adjusts the threshold level. The output of this stage is fed to the emitter of Q_5. It is in this stage that the strobing is done, the strobe pulse being fed through capacitor C_6 to the base of Q_5.

When the amplifier is quiescent, the collectors of Q_1 and Q_2 are biased at approximately - 3 volts. Potentiometer RV1 is adjusted such that the voltage at the common emitters of Q_3 and Q_4 is large enough to reverse bias them. The voltage at the common collectors will thus be -6 volts. This is directly coupled to the emitter of Q_5. The resistances R_9 and R_{10} are chosen such that the base of Q_5 is held at -2 volts. Thus Q_5 is reverse biased and its collector potential is -9 volts.

A differential signal applied to the bases of Q_1 and Q_2 causes the collector potential of one of the transistors to go more negative and that of the other transistor to go more positive. If the negative going signal is large enough to overcome the reverse bias set by RV1, one of the transistors Q_3 or Q_4 will conduct and the common collector potential will rise to approximately - 3 volts. In the absence of a strobe pulse, Q_5 will still be reverse biased and no output will be produced. A negative strobe pulse causes diode D_1 to cutoff and Q_5 becomes forward biased. The collector potential swings from -9 volts to the emitter potential of approximately -3 volts.

The detailed design of the sense amplifier is given in Appendix I.

5.3 Current Drive Amplifiers :

The current drive amplifiers supply the current pulses to the storage array. Half drive pulses for coincidence systems range from about 200 ma to 600 ma, depending on the type of core. The current drive amplifier is essentially a switch which switches the required current into the selected line. Ideally, this switch should be capable of switching rapidly and efficiently. Because of the low saturation impedance in transistors, it is possible to pass relatively large currents with low power dissipation in the transistor. Since current gain and speed are also desirable, the transistor should not be operated too far into saturation. A rise time of less than about a quarter of the switching time of the core is required. The ideal operating point would be at the knee of the grounded base - collector characteristic. This would assure low storage and low dissipation but would still provide full current gain.

One factor which must be given prime consideration in the design of the current drive amplifiers is the back e.m.f. generated by the stack. The magnitude of the back e.m.f. arising from the stack depends on the number of half selected cores, the pulse rise time and the inductance and resistance of the wire threading the core

The back e.m.f. is given by :

$$V_b = L \frac{dIr}{dt} + RI_r + WuV_1 + (\sqrt{N}\, W-W)\, r\, V_{h1}$$

Where : I_r = Read current

R = Resistance per unit length of drive wire

L = Inductance per unit length of drive wire

W = Word length

N = Number of words

rV_{h1} = Half read disturb '1' output

uV_1 = Full read undisturbed '1' output

This back voltage is of particular importance in transistor drive circuits where maximum permissable inverse voltage and power dissipation will set a limit to the size of stack that can be driven. Fig. 5.3 illustrates the effect of back e.m.f. on the driving current waveform. During the switching of the cores, the drive current dips. At the conclusion of the switching, the current returns to its limiting value. The cores are left in a state of saturation determined by the limiting value of the current. Thus during the application of the pulse the impedance of the stack varies considerably. In order to avoid some of the problems which arise from the changing load it is sometimes necessary to insert terminating impedances which match the impedance of the drive wires. The drive wires are delay lines and have a characteristic impedance approximated by $\sqrt{L/C}$, where L and C represent inductance and capacitance per unit length. The value of this characteristic impedance lies between 100 and 250 ohms depending on the type of core and wiring configuration. Provided that the wires are correctly terminated, the inverse e.m.f. will be of the same form as the drive current pulse so

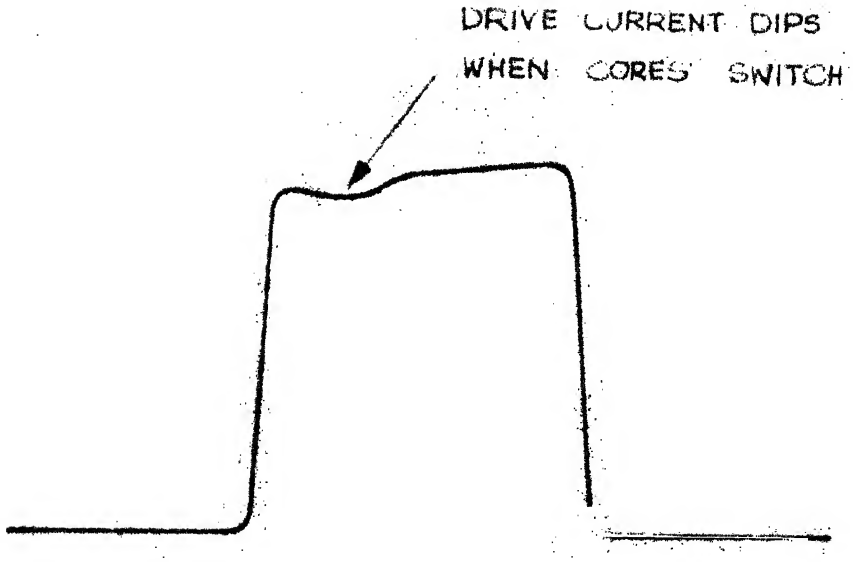


FIG. 5·3 EFFECT OF BACK E.M.F.

that the voltage drop across the line and the terminating resistor will be constant during most of the pulse. This enables drive circuits to be designed more easily and allows a voltage drive to be employed if desired.

Since a large amount of current, about 500 ma, is needed, the output transistor of the current driver amplifier would normally be operated in the grounded emitter configuration resulting in a current gain of about 30. However, the grounded emitter configuration, because gain is present, reduces the frequency response of the unit. The other alternative is to operate the output stage as a grounded base circuit. This has the advantage that it has a much better frequency response and would thus give a much better rise time. In addition, the grounded base circuit by virtue of its high output impedance, approximates a good current source thereby having the ability to withstand large back voltages. The main disadvantage is that no current gain exists. In effect then, the grounded base stage is used as an isolation stage having unit current gain.

In view of the small memory size and consequent small back e.m.f. that would be encountered, a grounded emitter output stage was decided on. The complete circuit is shown in Fig. 5.4. The same circuit could be used for larger systems by merely incorporating a grounded base stage between the output stage and the drive lines and no additional modification to this circuit is required.

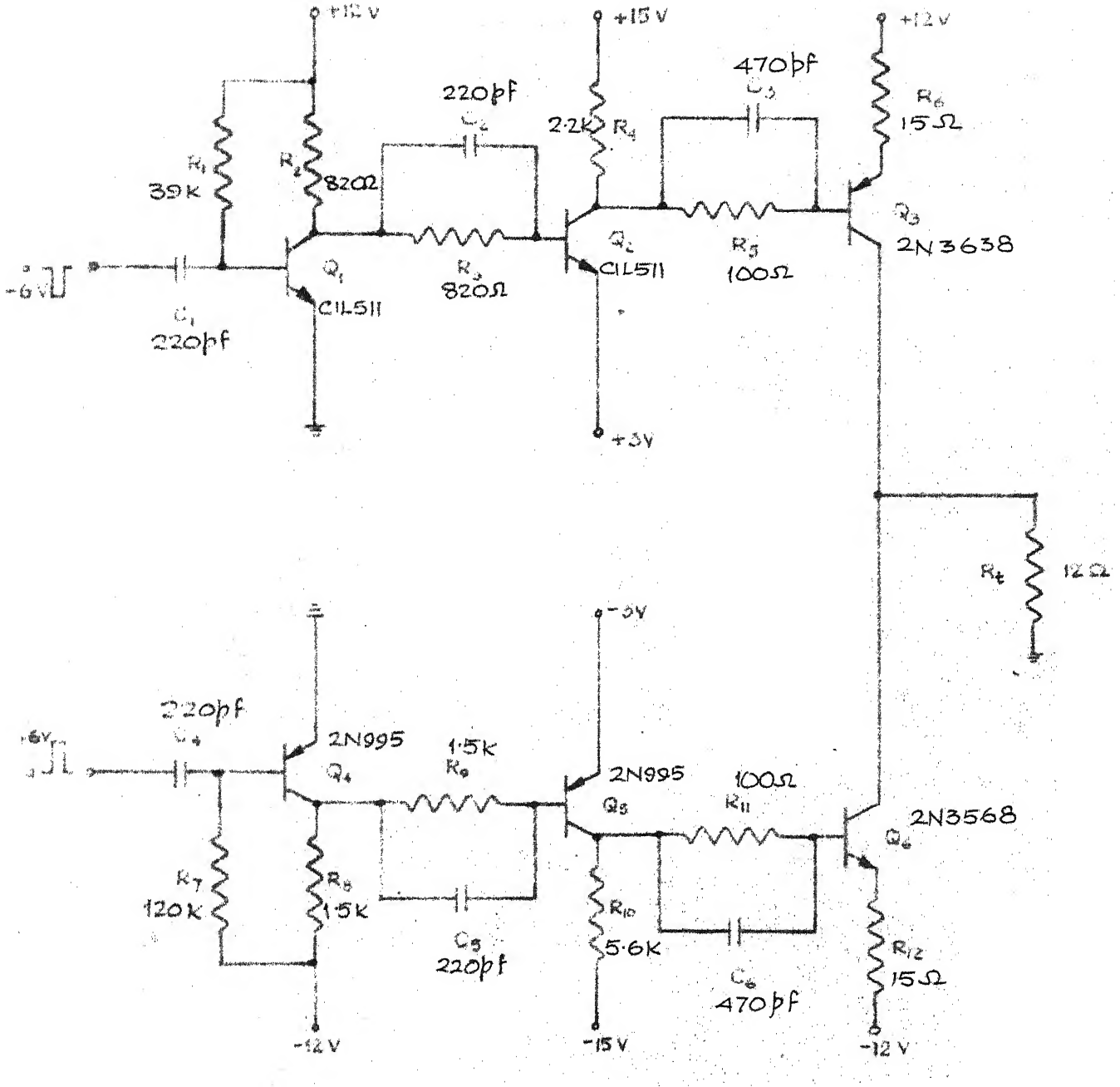


FIG 3·4 READ/WRITE CURRENT DRIVE AMPLIFIER

Description of the Circuit :

The current driver amplifier consists essentially of two parts - the positive current driver and the negative current driver. The operation of these two parts is exactly the same. Consider the positive current driver. In the quiescent condition, Q_1 is conducting and its collector voltage is low enough to reverse bias the base emitter diode of Q_2. Consequently, Q_2 is cutoff and its collector voltage is essentially equal to the supply voltage. This in turn reverse biases the base emitter diode of the driver transistor Q_3, which is also held at cutoff. A negative pulse applied to the base of Q_1 cuts off this transistor. Its collector voltage rises to the supply voltage thereby forward biasing the base emitter diode of Q_2. The collector voltage of Q_2 drops to the emitter voltage and Q_3 whose base emitter diode is now also forward biased, conducts heavily. Sufficient base drive is supplied to Q_3 to saturate it. Under these conditions, the collector current of Q_3 is limited only by the supply voltage and the resistances R_t and R_6. Thus by varying R_6 the current can be set to the desired value - in this case 400 ma.

The operation of the negative current driver comprising Q_4, Q_5 and Q_6 is exactly the same. The detailed design of the current driver amplifier is discussed in Appendix II.

5.4 The Line Selection Driver :

The simplest arrangement for driving the X and Y lines of a coincident drive store consists of a pair of transistors

on each line. These two transistors are required to supply the positive and negative drive pulses. For a large store this becomes very uneconomical. An economy in hardware can be achieved by deriving the drive pulses from a common drive circuit and routing them into the required X and Y lines through a pair of bidirectional gates. The selection of one gate on each of the X and Y lines is done by the decoder.

The main problem associated with the design of this gate is that the decoder output, which is a voltage level of one polarity, must be able to select a gate which can pass current pulses of both polarity. In addition, when the gate is not selected, both current pulses must be completely blocked. The simplest arrangement would be to use a bidirectional transistor or a transformer with two output coils suitably would. These two schemes are shown in Figs. 5.5a and 5.5.b, However, the unavailability of these components precludes their use. The circuit of Fig. 5.6 shows a bidirectional gate in which diodes D_1, D_2, D_3 and D_4 in conjunction with Q_3 effectively simulate a symmetrical transistor.

Description of the Circuit :

Transistors Q_1 and Q_2 supply the necessary base current to Q_3 to turn it on. The decoder output is directly coupled to the base of Q_1. In the quiescent condition, Q_1 is cutoff and its collector is held at the supply potential. This reverse biases Q_2 which in turn holds Q_3 in cutoff. The reverse bias on Q_3 is large enough so that a potential of +6 volts appearing on the emitter is not large enough to make it conduct. Diode

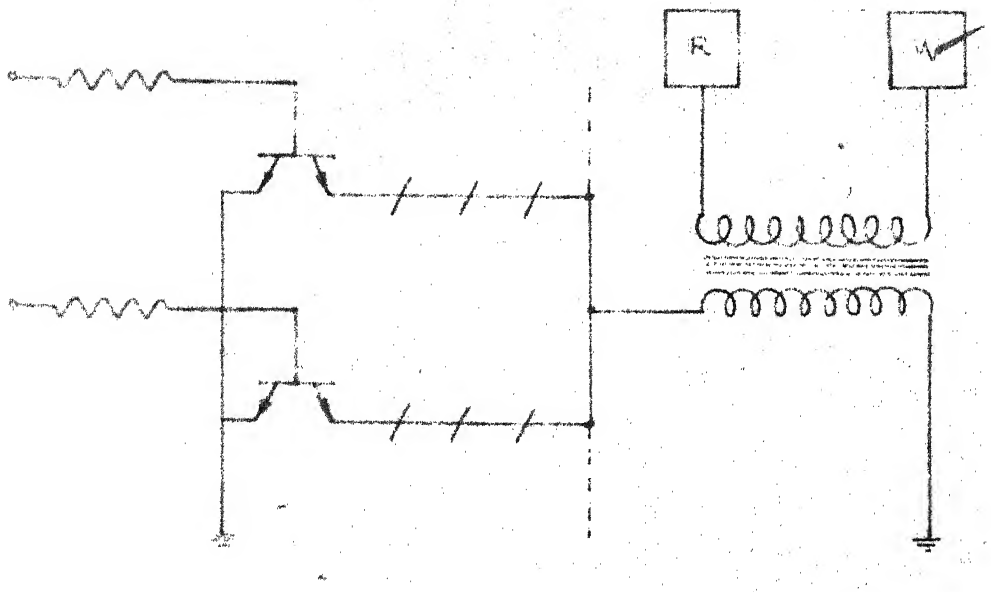


FIG 5.5A DRIVE WIRE SELECTION USING SYMMETRICAL TRANSISTORS

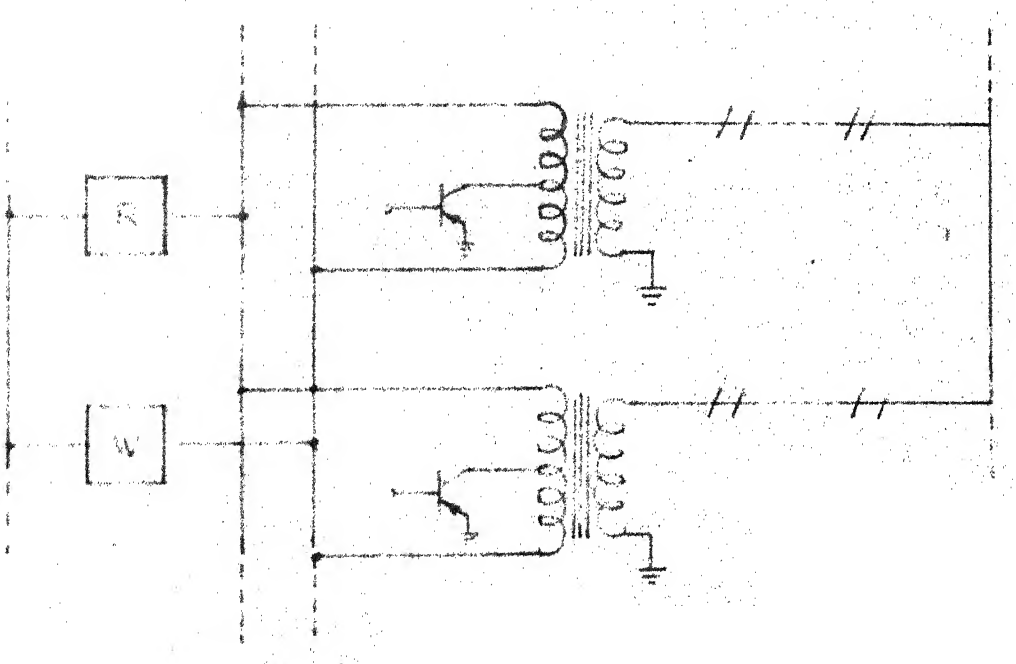


FIG 5.5B DRIVE WIRE SELECTION USING TRANSFORMERS

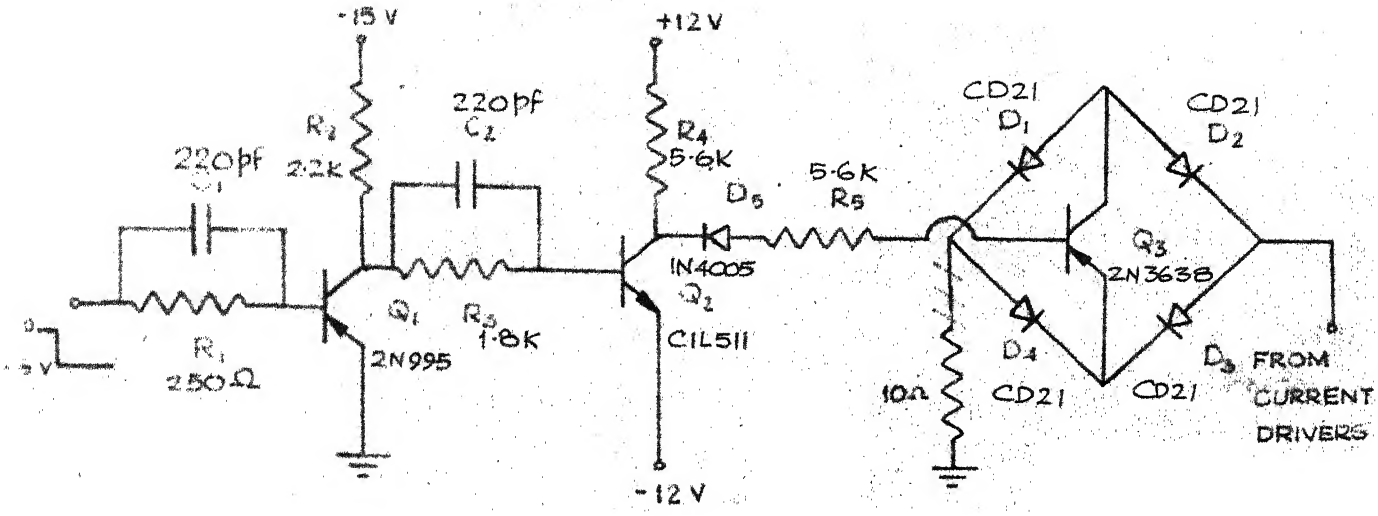


FIG 5.6 LINE SELECTION DRIVER

D_5 is chosen to have a very small reverse leakage current as compared to the base emitter diode of Q_3. This is necessary since the reverse breakdown of the base emitter diode of Q_3 is +5 volts.

When Q_3 is turned on, sufficient base current is supplied so that a negative current can be routed through diodes D_2 and D_4, and a positive current through diodes D_1& D_3 into the 10 ohms terminating resistance.

The complete design of circuit is given in Appendix III.

5.5 The Decoder :

The decoder is required to decode the contents of the Memory Address Register and select the appropriate X and Y drive lines. Each output from the decoder is a different minterm and may be fed directly to a load.

A number of possible schemes exist. Consider first the development of all minterms in a 1-level form. This development requires 'n' diodes for ANDing the 'n' variables in a given minterm. Since there are 2^n different minterms, the total number of required diodes is

$$N_d = n2^n$$

The corresponding array is called a 'rectangular matrix'. An example of a four variable matrix is shown in Fig. 5.7.

If a matrix is not limited to a single stage for each output, the iterative subfunctions among a complete set of minterms can be exploited. For example, a 'b' is required for both a 'b' 'c' and a 'b'c in a three variable set. Thus, a

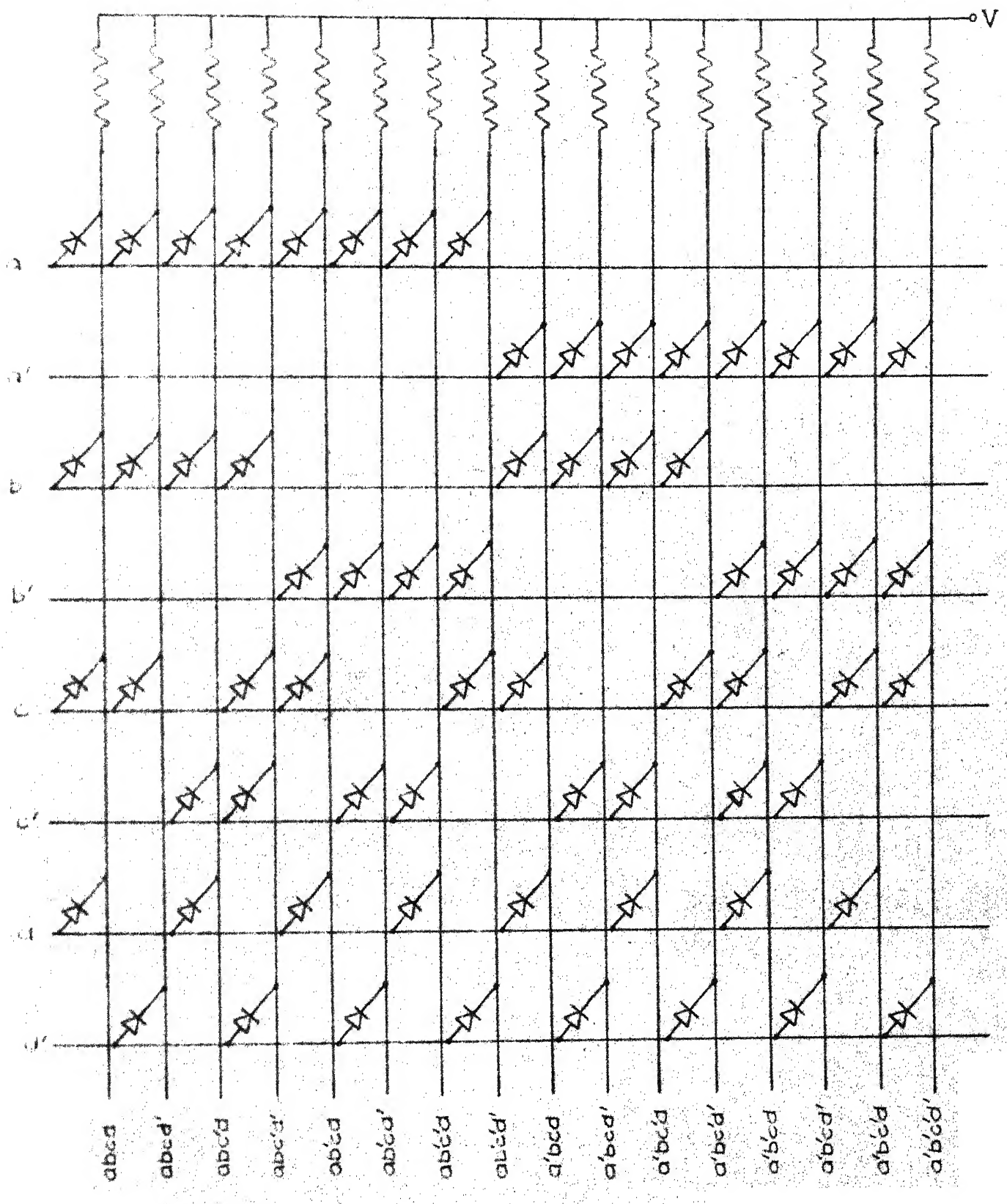


FIG 5.7 RECTANGULAR MATRIX

matrix may be formed by first generating all combinations of two variables in the fashion of a rectangular matrix. Then, in a second stage, the first set of combinations are combined exhaustively with a third variable. In a third stage, these combinations are combined exhaustly with a fourth variable and so on until finally at stage n-1, all variables have been used and all minterms have been generated. Such a matrix is called a 'pyramid', a four variable example of which is illustrated in Fig. 5.8. The total number of diodes required for this matrix is

$$N_d = 2^{n+2} - 8$$

The pyramidal matrix does not fully exploit the iterations among the minterms. For example, in a four variable set of minterms it is more economical to form all a, b combinations, then separately form all c, d combinations, and then combine these subcombinations. A matrix of this type is called a 'sectional matrix ' and a four variable form is shown in Fig. 5.9. The number of diodes is given by :

$$N_d = 8N_2 + 24N_3 + 2 \left(\sum_{b=1}^{m} N_b \right) + 2^{n+1}$$

Where N_2 = Number of two variable sets

N_3 = Number of three variable sets

N_B = Number of outputs from intermediate bank numberb.

m = Number of intermediate banks

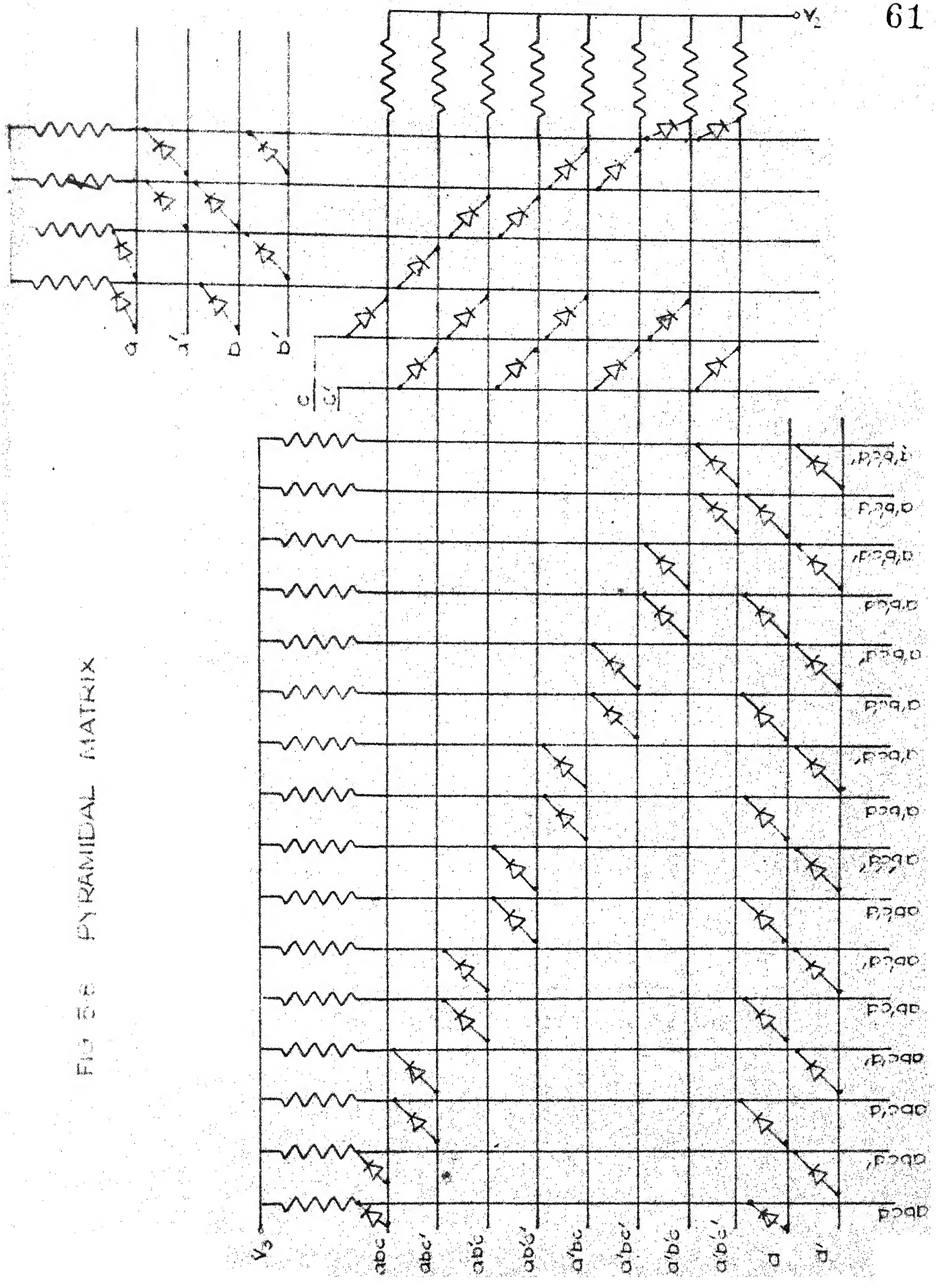
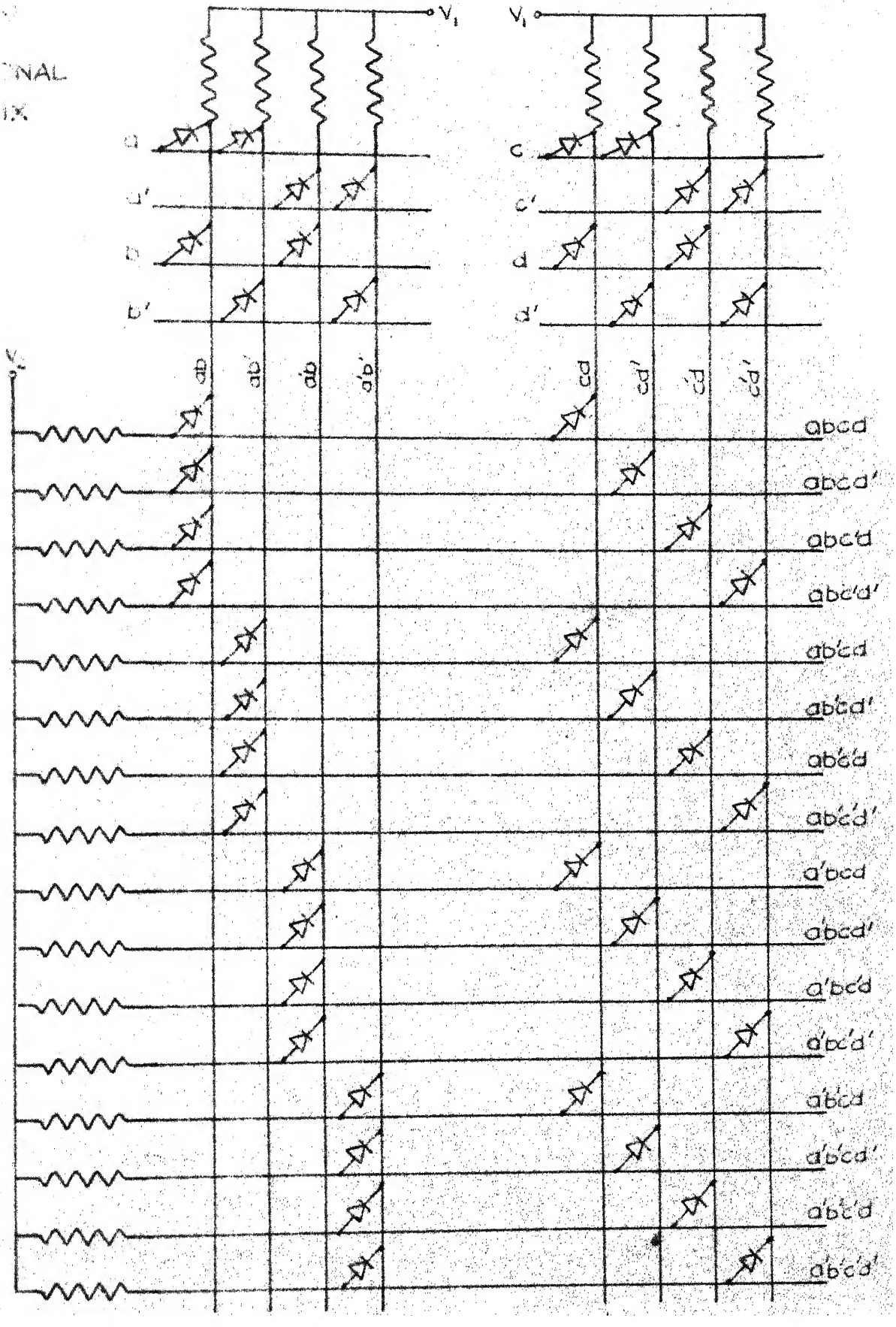


FIG 16.8 PYRAMIDAL MATRIX

FIG 5-1

SECTIONAL MATRIX



For each of the matrices, the number of diodes required is

1. Rectangular matrix 64 diodes
2. Pyramidal matrix 56 diodes
3. Sectional matrix 48 diodes

Thus, as expected, the Sectional matrix requires the least number of diodes. However, the difference is not great.

The Rectangular matrix was chosen for two main reasons. Firstly, since it requires only a single level of gating, its speed of operation is faster. Secondly, for a small number of variables the Rectangular matrix proves to be cheaper. This results from the fact that since the Pyramidal and Sectional matrices have more than one level of gating, higher voltage supplies are required at each successive level to maintain a good rise time. The cost of extra diodes in the Rectangular matrix is more than compensated for by the cost of additional power supplies in the Pyramidal and Sectional matrices.

The basic circuit for the Rectangular matrix is the four input AND gate shown in Fig. 5.10. The design of this circuit is given in Appendix IV.

5.6 The Parity Check Circuit :

The parity check circuit is incorporated as part of the main memory system to ensure reliable operation. The function of the circuit is to detect the loss of a single bit during the transmission of a word from the memory stack to the MBR. The loss of an even number of bits will however, not produce a parity error.

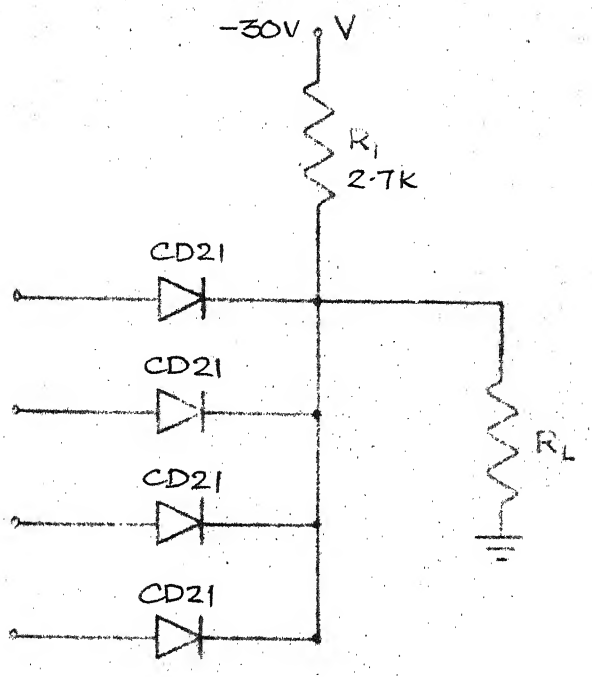


FIG 5.10 FOUR INPUT 'AND' GATE

The circuit is required to operate both during the READ/RESTORE and CLEAR/WRITE modes of operation. In the CLEAR/WRITE mode the number of logic '1' bits in the word to be stored are checked. If the number of bits is odd, an extra bit must be added in the appropriate bit position in the MBR. If however, the number of bits is even, no action is taken. Therefore, any word stored in the memory must have an even number of logic '1' bits.

In the READ/RESTORE mode, the parity check circuit operates after the required word has been read from core storage and is stored in the MBR. During transmission, if an odd number of bits are lost, the MBR will contain a word with an odd number of logic '1' bits. This error is detected by the parity check circuit which sets the parity check flip flop. The CPU interrogates this flip flop during every memory cycle to check for parity errors.

The basic module of the parity check circuit is the 'exclusive OR' gate. These are connected to the MBR as shown in Fig. 5.11. When an odd number of flip flops in the MBR are set the output line is energised.

The transmission function for the 'exclusive OR' gate is :

$$T = A\bar{B} + \bar{A}B$$

A direct hardware realisation of this would require two AND gates and one OR gate. Such a direct realisation has two main disadvantages. Firstly, since there are no active elements, the output will not be well defined. Secondly, the circuit

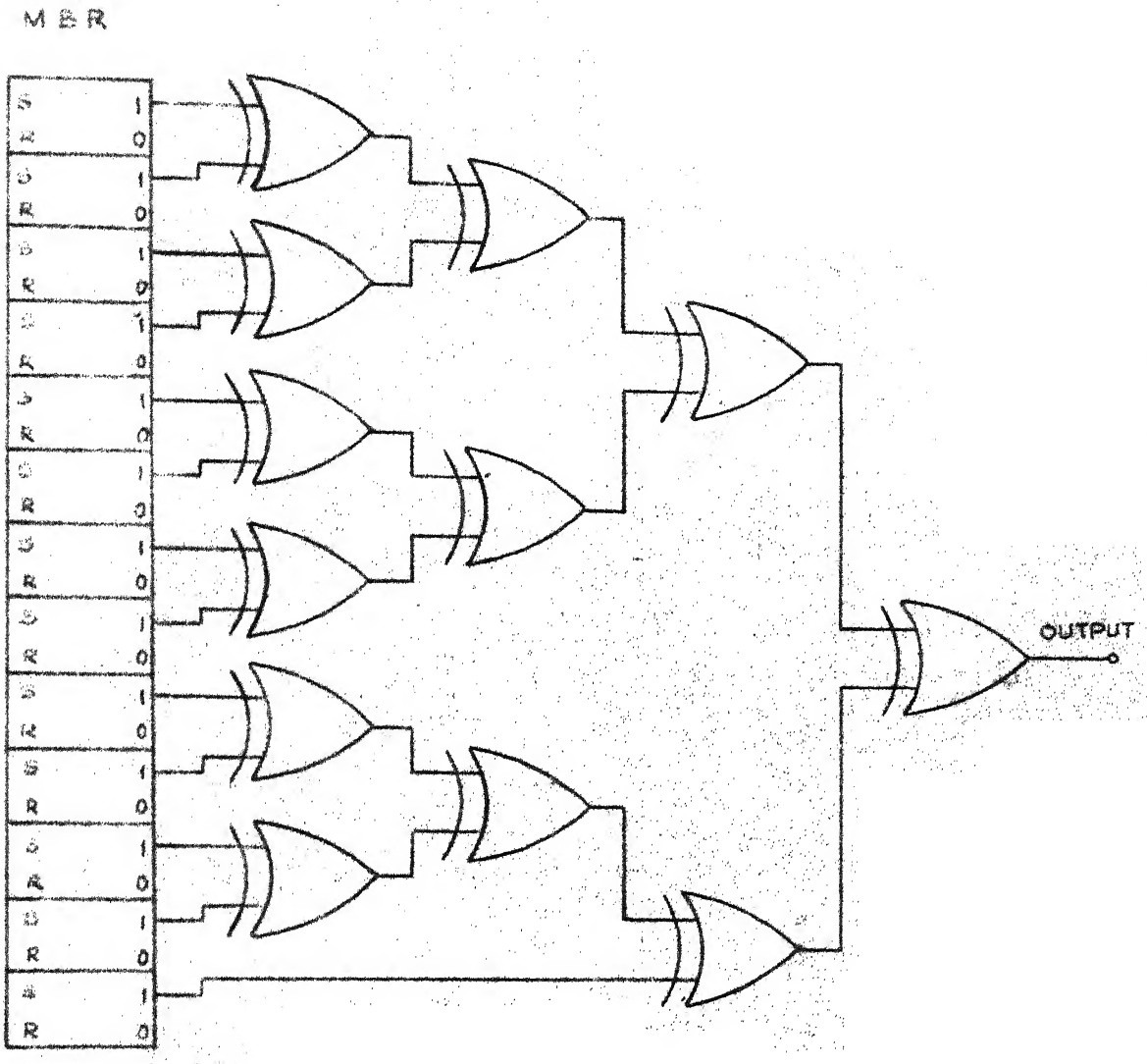


FIG 5·11 PARITY CHECK CIRCUIT

action would be slow due to the multi level gating. In order to obtain a good rise time, successively higher voltage would be required at each level of gating. A transistor circuit which performs the 'identity' function and can be used for parity checking is shown in Fig. 5.12.

Description of the Circuit :

The input terminals A and B of the circuit of Fig.5.12 are connected to the output terminals of two flip flops of the MBR. When the two flip flops are both either set or reset, the base to emitter drop of Q_1 and Q_2 will be approximately zero. Consequently, both transistors will be cut off and the output point C will be held at -6 volts. On the other hand, if one of the flip flops is set and the other reset, one of the transistors conducts and the output falls to approximately ground potential. The truth table for this circuit can now be constructed:

A	B	C
0	0	-6
-6	0	0
0	-6	0
-6	-6	-6

The circuit can be realised conveniently by modifying the two input TRL NOR gate. This is discussed in Appendix V.

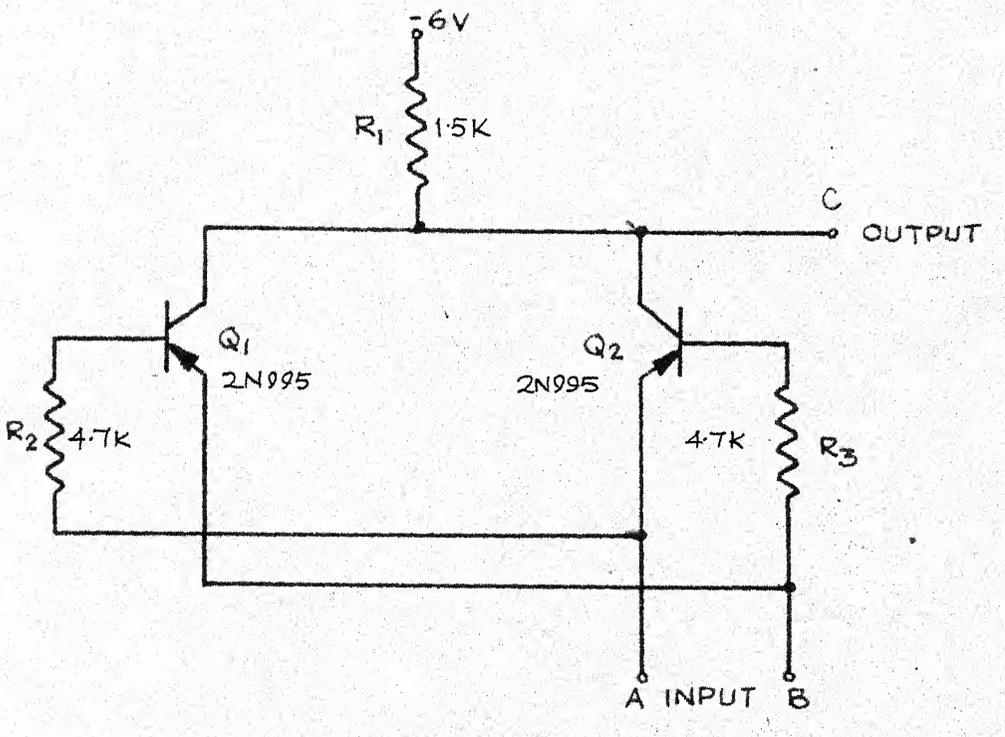


FIG 5 12 IDENTITY ELEMENT

CHAPTER VI

MEMORY TIMING

6.1 Memory Timing

The memory system has two modes of operation : READ/RESTORE, in which the information stored in a given address is read and then restored in the same location; and CLEAR/WRITE in which information in an address location is erased by a read operation and new information is written in that location.

On receipt of a READ/RESTORE or CLEAR/WRITE command and an initiate command, the timing generator automatically generates the required accuretely timed pulses for a single memory cycle. For both modes of operation the same pulse pattern is generated. The Memory Control circuitry routes the pulses to various points depending on the mode of operation. The switching time of the cores in the storage array determines to a large extent the length of the memory timing signals and the duration of the reading and writing signals. Fig. 6.1 shows the various pulses generated by the timing generator in their proper time sequence. The seven command pulses are :

(i) Clear MBR and parity check flip flop - M_T

(ii) X, Y Read - R_T

(iii) Data Strobe - S_T

(iv) Check Parity - P_T

(v) X, Y Write - W_T

(vi) Inhibit Control - I_T

(vii) Op Complete - O_T

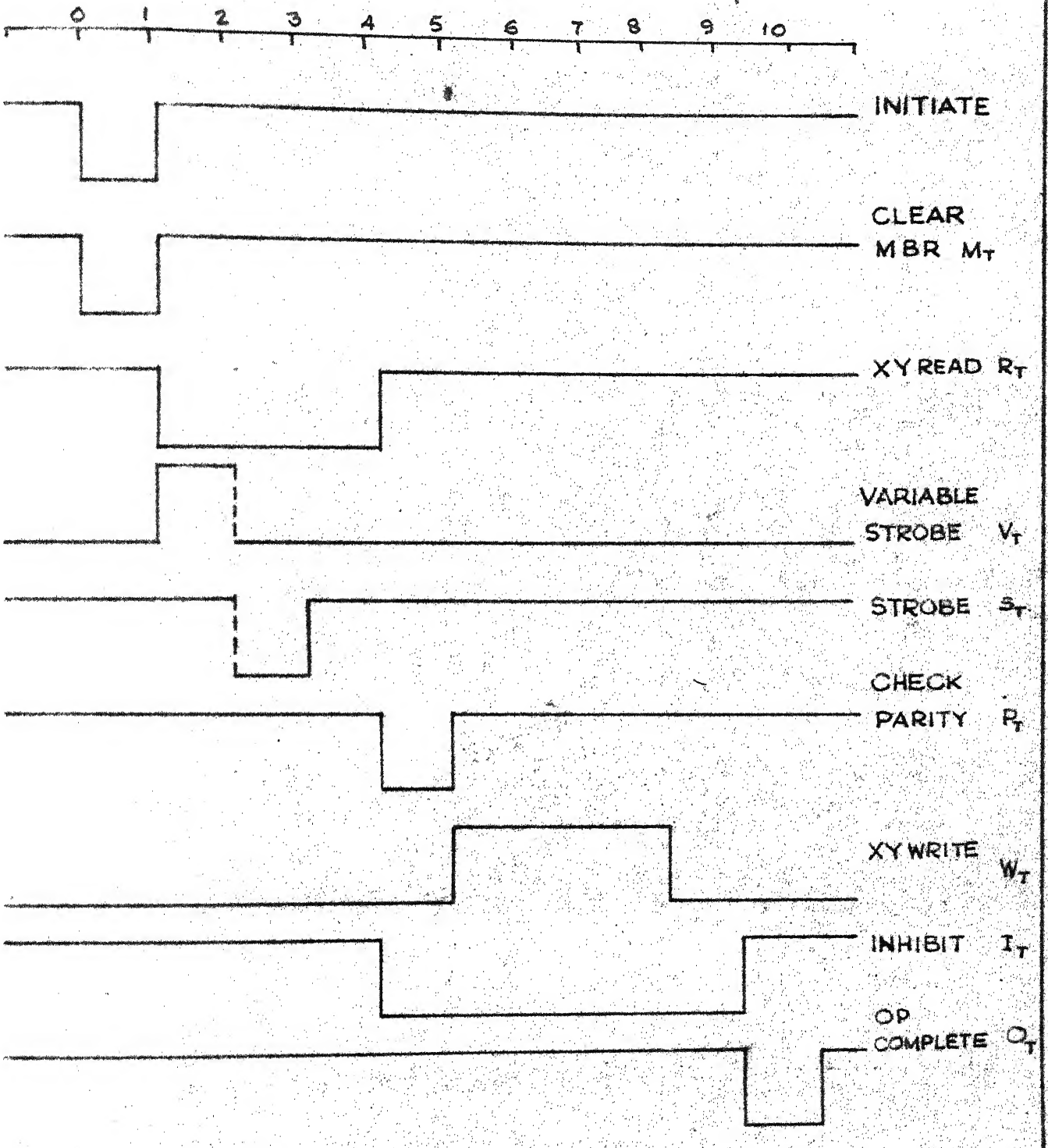


FIG 6-1 MEMORY COMMAND PULSES

Command pulse M_T resets the MBR thus clearing information that had been entered into it as a result of a previous cycle. This pulse is routed to the reset terminal of the MBR only during a READ/RESTORE cycle, since information which is to be stored into the memory during a CLEAR/WRITE cycle is stored in the MBR. In addition, the command pulse M_T is applied to the reset terminal of the parity check flip flop. This is necessary to ensure that the CPU does not halt as a result of a parity error in a previous cycle. The parity check flip flop is interrogated by the CPU during every memory cycle to check for parity errors.

Command pulse R_T is the X, Y READ command, which triggers the read current drivers. The width of this pulse is dependent on the switching time of the cores, which in this case is 3 microseconds. The read current is routed to the proper group of cores in the core matrix through the line selection drivers which are selected by the decoders. When the ferrite cores are switched, the generated voltage is applied to the sense amplifiers. During the X, Y Read command, a command pulse S_T of duration 1 microsecond, is generated to gate the data from the core matrix to the MBR. This command pulse is preceeded by a pulse V_T, whose width can be manually varied. The width is adjusted so that S_T is generated at the time of maximum signal to noise ratio. During a CLEAR/WRITE cycle, S_T is blocked from the input to the sense amplifiers, since, during this mode of operation, the X, Y Read pulse is

used to clear the location into which new information is to be written. At the termination of the X, Y Read pulse a 1 microsecond wide parity check pulse, P_T, is generated. This pulse performs different functions during the READ/RESTORE and CLEAR/WRITE modes of operation. In the READ/RESTORE mode, P_T is gated with the output of the parity check circuit to the set terminal of the parity check flip flop. The occurrence of a parity error causes P_T to set this flip flop and the CPU terminates further processing. In the CLEAR/WRITE mode of operation, P_T is gated with the output of the parity check circuit to the appropriate flip flop of the MBR which stores the parity bit. The word to be written into the memory is initially stored in the MBR. Its parity is checked by the parity circuit. If the required parity is not satisfied, P_T sets the flip flop in the MBR.

After data from the core matrix has settled in the MBR, command pulses I_T and W_T are generated simultaneously. The command pulse W_T is the X, Y Write command which triggers the X, Y write current drivers. The write current pulse of 3 microseconds duration is routed to the same group of cores from which information was read. This pulse is of sufficient magnitude to switch the proper group of cores back to the logic '1' state. To store information other than a logical '1' in the core matrix, the Inhibit control pulse I_T, triggers the Inhibit current drivers, which, in association with the data present in the MBR generate a current sufficient in magnitude to oppose the switching of the selected group of cores. That is to say,

when a logical '0' is to be stored in a particular location, the associated Inhibit driver is turned on, neutrialising the effect of the switching pulse on the core. The Inhibit control pulse overlaps the write current pulse on both the leading and trailing edges to prevent false switching of the cores. This completes the memory cycle and the last command pulse, O_T, is generated as the Operation complete signal. This pulse is routed directly to the control circuitry in the CPU.

6.2 The Command Pulse Generator :

The complete block diagram of the command pulse generator is given in Fig. 6.2. It consists essentially of a series of monostable multivibrators. The output of each monostable is connected to the input of the succeeding monostable. This effectively forms a delay line from which tappings can be taken at the appropriate points to obtain the desired command pulses at the specified time intervals. The first monostable is triggered by the lockout flip flop, FF1. This flip flop is set by an initiate pulse from the CPU or a pulse from monostable SS13, by depressing the manual start button. The two AND gates are fed at one input from the complementary outputs of the AUTO/MANUAL flip flop. This prevents interference between the MANUAL and AUTOMATIC modes of operation of the memory. An initiate pulse either from the CPU or manually, causes the lockout flip flop to set. A second initiate pulse occuring before the completion of one memory cycle will thus have no effect. The output of this flip flop triggers SS2,

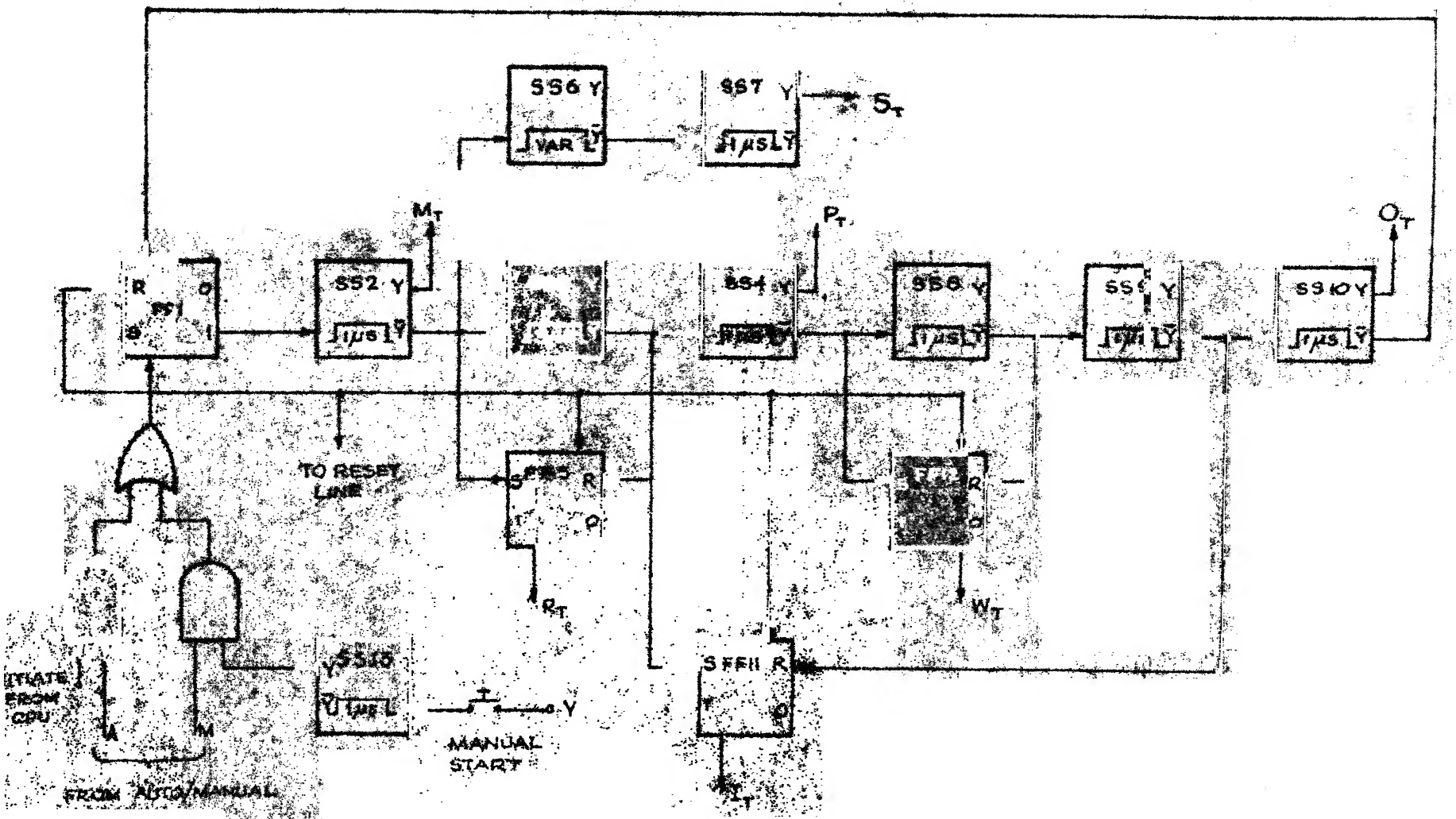


FIG 5-2 COMMAND PULSE GENERATOR

whose output is the command pulse M_T. The termination of this pulse causes SS3 and SS6 to trigger. The trailing edge of the pulse from SS2 sets FF5. SS6 provides the variable delay to trigger SS7 which generates the command pulse S_T. The output of SS4 is the command pulse P_T. The trailing edge of the output from SS3 resets FF5 and sets FF11. FF5 generates the command pulse R_T. Similarly the command pulse W_T is generated by FF12. The output of SS10 is the command pulse O_T. The trailing edge of the output from SS9 resets FF11 which generates the command pulse I_T. The output from SS10 resets the lockout flip flop in preparation for the next memory cycle. Since the switch on state of the lockout flip flop is not known, a manual reset line is provided. This line must be activated immediately after switch on, before the memory is operated in the automatic mode.

Fig. 6.3 shows how the command pulses are derived from the timing generator waveforms.

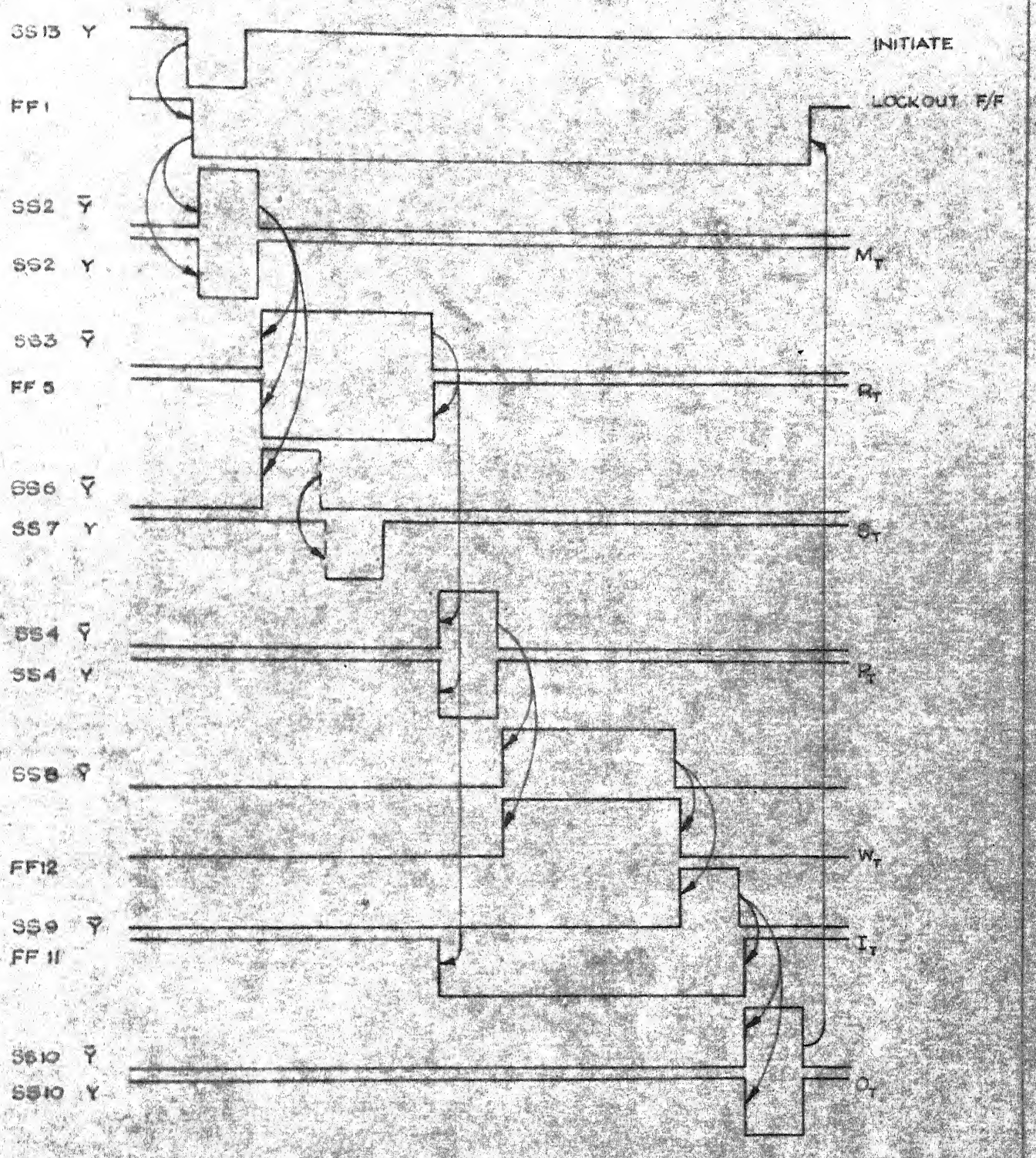


FIG 6.3 DERIVATION OF COMMAND PULSES

CHAPTER VII

THE DETAILED BLOCK DIAGRAM

7.1 AUTO/MANUAL and READ/WRITE Circuitry :

The full cycle of the memory has two modes of operation : READ/RESTORE and CLEAR/WRITE. It may be operated in either of these modes in automatic status or manual status. In the automatic status (AUTO), all inputs and outputs from the memory are performed under control of the CPU. In the manual status (MANUAL), these operations may be performed manually through sets of switches located on the front panel. In order to prevent any false operation it is necessary to isolate the manual entry switches when the memory is in AUTO status, This is accomplished by the circuitry of Fig. 7.1 Flip flop FF1 stores information regarding the mode of operation - READ/RESTORE or CLEAR/WRITE. Flip flop FF2 puts the memory in AUTO or MANUAL Status. The state of FF2 is set by switch S1. The state of FF1 is set by the outputs of the AND gates R_A and W_A or by the AND gates R_M and W_M at the D.C. set terminals.

With switch S1 in the MANUAL position, output terminal M of FF2 is at a potential V, and the output terminal A, is virtually at ground potential. Consequently, the AND gates W_A and R_A are disabled and the gates W_M and R_M are enabled. Depressing the push button switches P_W or P_R puts FF2 in the CLEAR/WRITE or READ/RESTORE mode. Depressing switch P_M energises the reset line to manually reset the various registers in the memory. In addition, the output terminal M of FF2 is fed

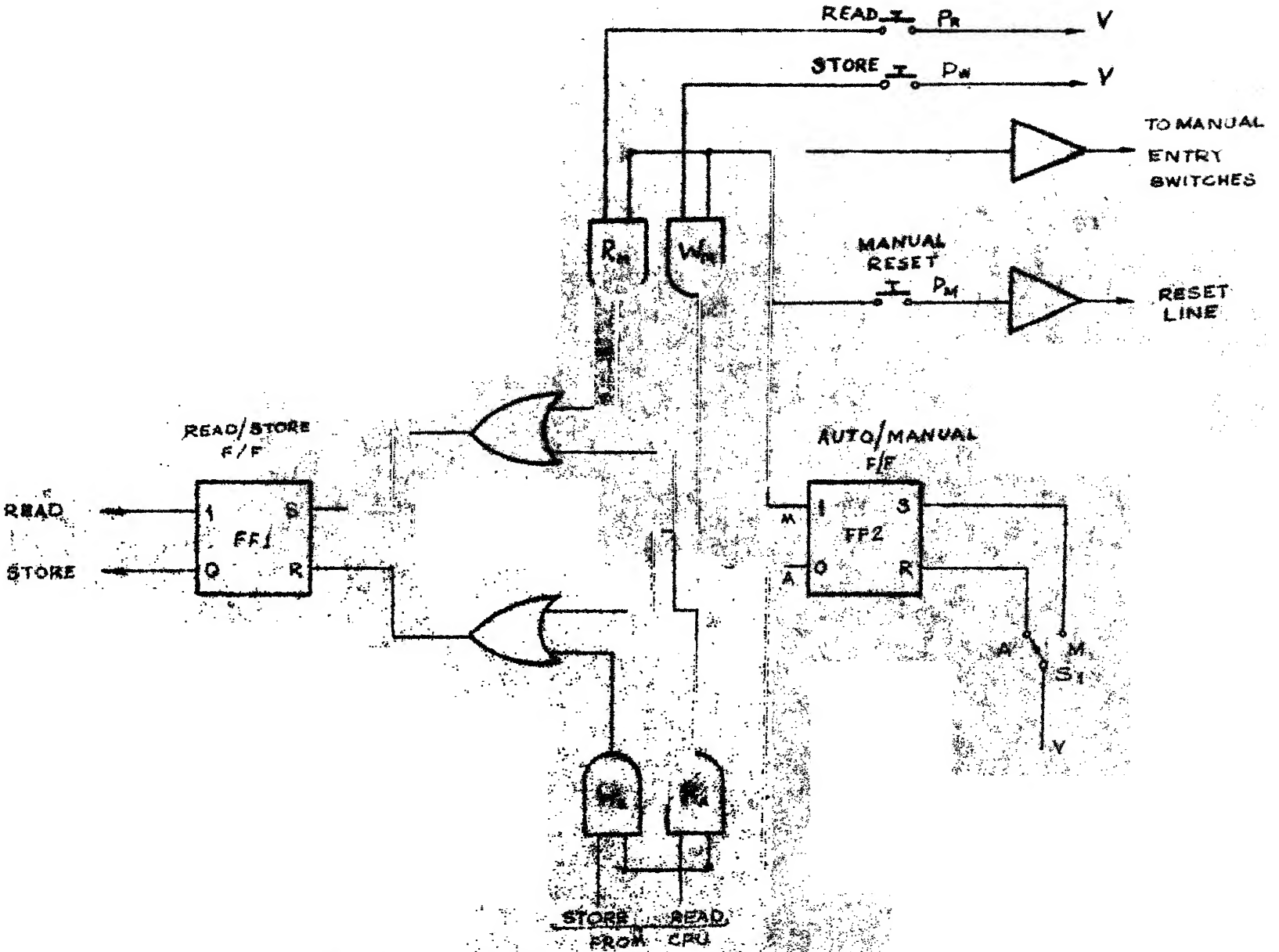


FIG 7.1 MEMORY CONTROL CIRCUITRY

to a non inverting buffer amplifier, whose output provides the voltage to the manual entry switches. When S1 is placed in the AUTO position the AND gates W_A and R_A are enabled. The circuitry associated with the MANUAL operation will now be ineffective since the output terminal M, will be virtually at ground potential. FF1 may now be set in the READ/RESTORE or CLEAR/WRITE mode by inputs from the CPU to the AND gates R_A or W_A.

7.2 The Memory Address Register Logic Circuitry :

The logic circuitry associated with the MAR is shown in Fig. 7.2. The set of OR gates permit an address to be set up in the MAR either manually through a set of manual entry switches or automatically under control of the CPU. The manual entry switches are a set of single pole double throw switches. One common line from all the switches connects to the supply voltage. The other common line is grounded. The output terminal M on the AUTO/MANUAL flip flop is connected to the common input line of the set of AND gates.

When the memory is in AUTO status, the AND gates are disabled and the contents of the MAR can be set by the CPU. In the MANUAL status, the AND gates are enabled and the CPU loses control. The logical '1' position of the manual entry switches now permits the appropriate flip flops of the MAR to be set manually. All the reset terminals of the flip flops are connected to a common line to enable the MAR to be reset automatically by the CPU or manually by depressing the manual reset switch.

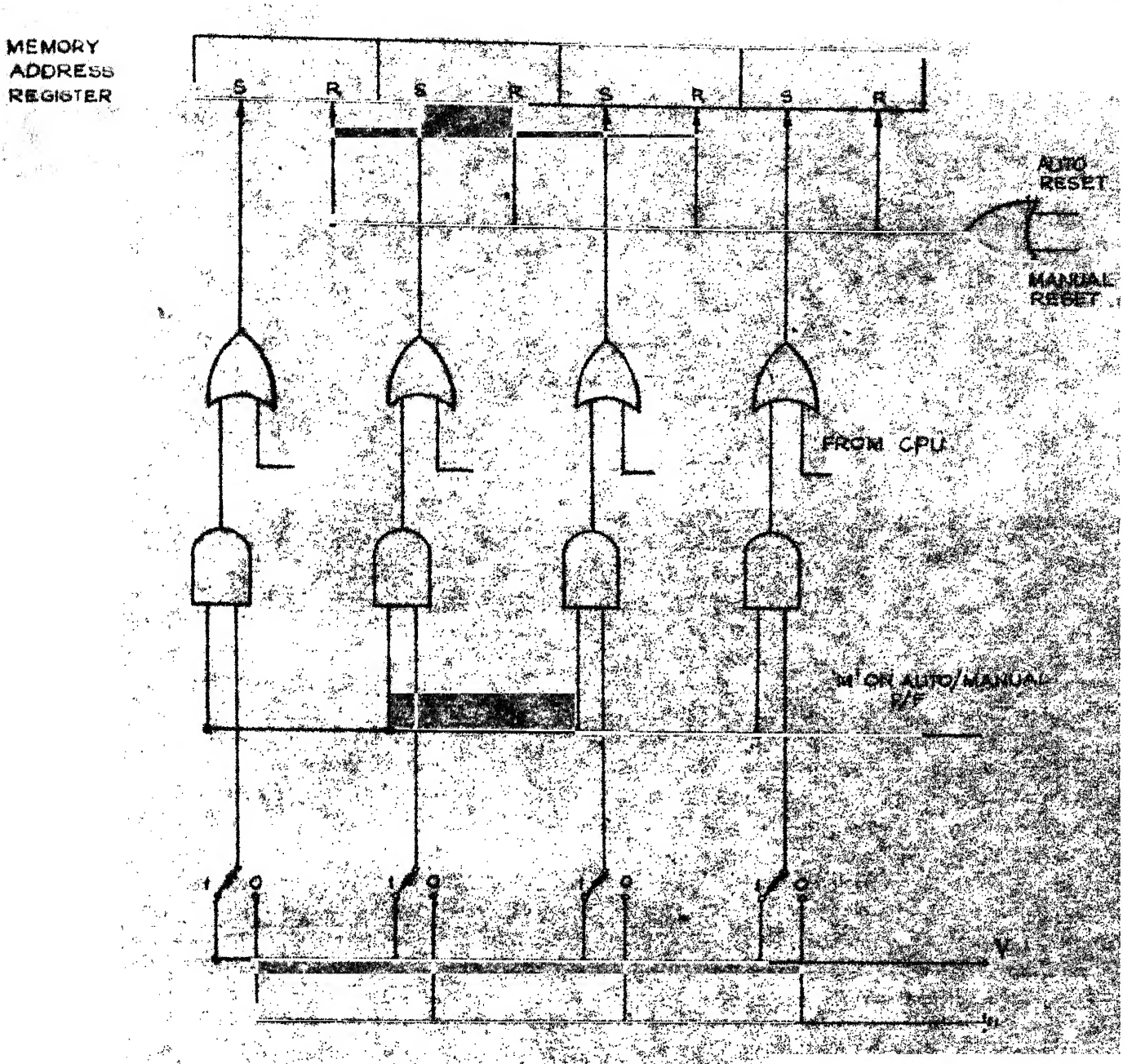


FIG. 7-2 MAR LOGIC CIRCUITRY

7.3 The Memory Buffer Register Logic Circuitry :

The logic circuitry associated with the MBR is shown in Fig. 7.3.

As with the MAR, facilities have been provided for manual entry of information. In the AUTO mode of operation, information to be stored in the memory is contained in the MBR. In the MANUAL mode, however, this information does not go into the MBR, but is set up directly in the manual entry switches. A set of OR gates present the information contained in the MBR or the manual entry switches to the inputs of a set of AND gates which pass the inhibit control pulses to the Inhibit current drivers. In the AUTO status, both terminals of each of the manual entry switches are effectively grounded. This is achieved by connecting the logical '1' position of switches to the output terminal M of the AUTO/MANUAL flip flop. The other terminals are grounded. In the MANUAL status, the information contained in both the MBR and the manual entry switches is presented to the inhibit drivers. However, before the beginning of a read cycle, the MBR is reset by command pulse M_T. This rather complicates the reset circuitry associated with the MBR. In the READ/RESTORE mode, command pulse M_T is to reset the MBR when the memory is in AUTO or MANUAL status. However, during the CLEAR/ WRITE mode, the MBR should be reset only in MANUAL status and not in AUTO stuatus. These conditions result in the logic circuitry of Fig. 7.4.

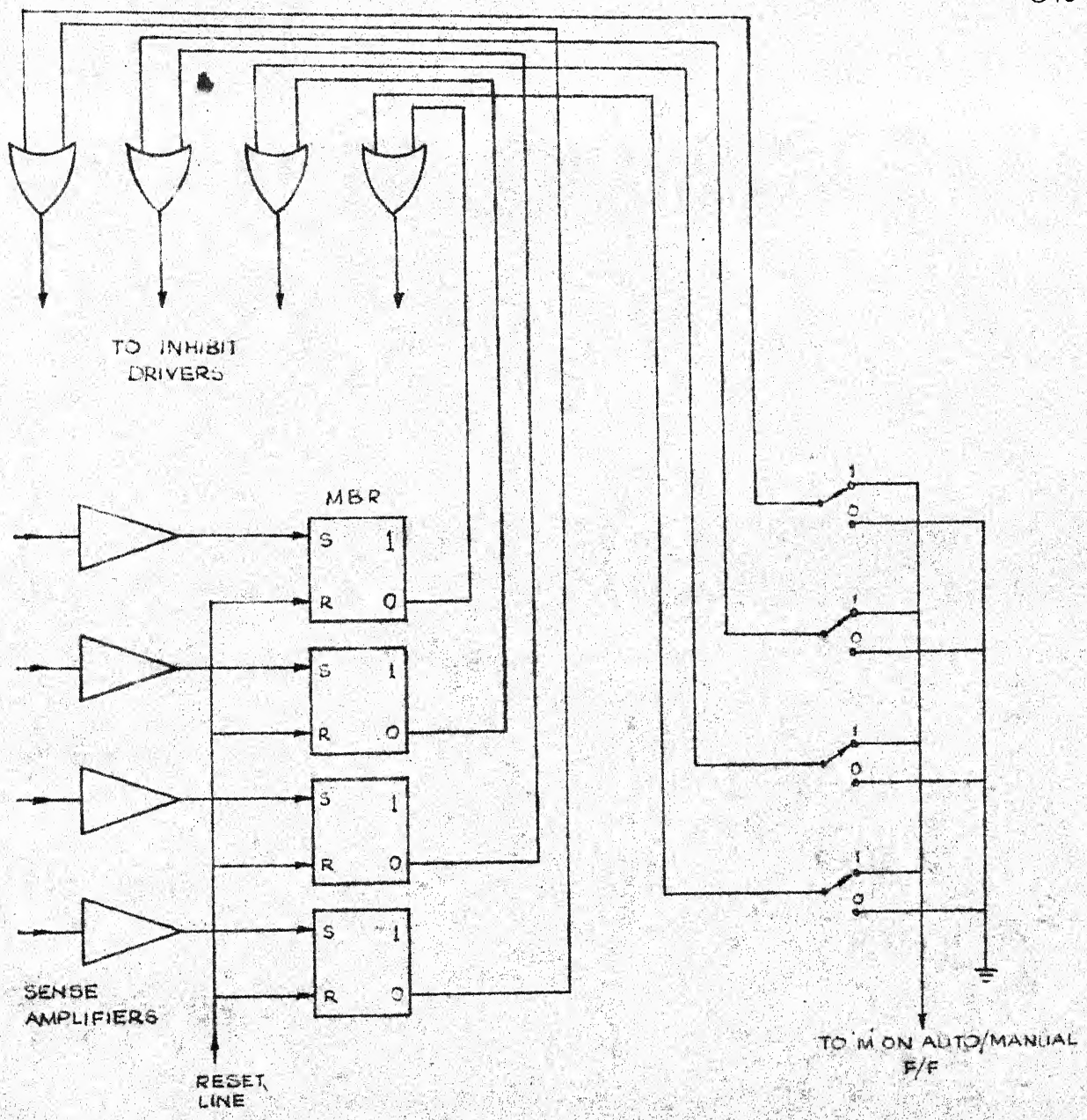


FIG 7·3 MBR LOGIC CIRCUITRY

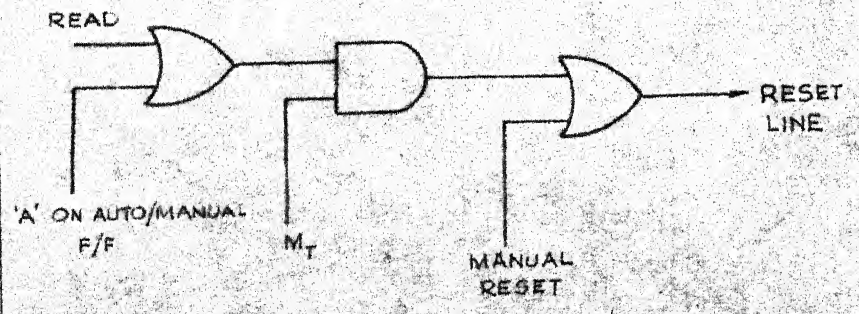


FIG 7·4 MBR RESET CIRCUIT

7.4 The Parity Check Logic Circuitry :

Fig. 7.5 shows the logic circuitry associated with the Parity checking circuit. The inputs to the circuit come directly from the MBR and the output feeds two AND gates. One of these gates is operative during the READ/RESTORE and the other during the CLEAR/WRITE mode.

The loss of a single bit during transfer of information from the memory stack to the MBR, causes a word of odd parity to be stored in the MBR. The parity check circuit produces an output which together with the input from the READ/RESTORE line causes the command pulse P_T to set the parity check flip flop. This flip flop is initially reset by the command pulse M_T. For no parity error, P_T is blocked at the AND gate. To allow for the ignoring of a parity error, the parity check flip flop may be reset automatically on command from the CPU or manually by depressing the manual reset switch.

In the CLEAR/WRITE mode of operation, the parity check circuit checks the parity of a word which may be stored in the MBR or in the manual entry switches. If the word does not have even parity, the output of the parity check circuit together with the input from the CLEAR/WRITE line causes the command pulse P_T to set the appropriate flip flop in the MBR. This flip flop is used only to store information regarding parity and its output is not avaialable to the CPU. In manual status although the Inhibit drivers are selected by information in the manual entry switches, the Inhibit driver associated with the parity bit is selected by the appropriate flip flop.

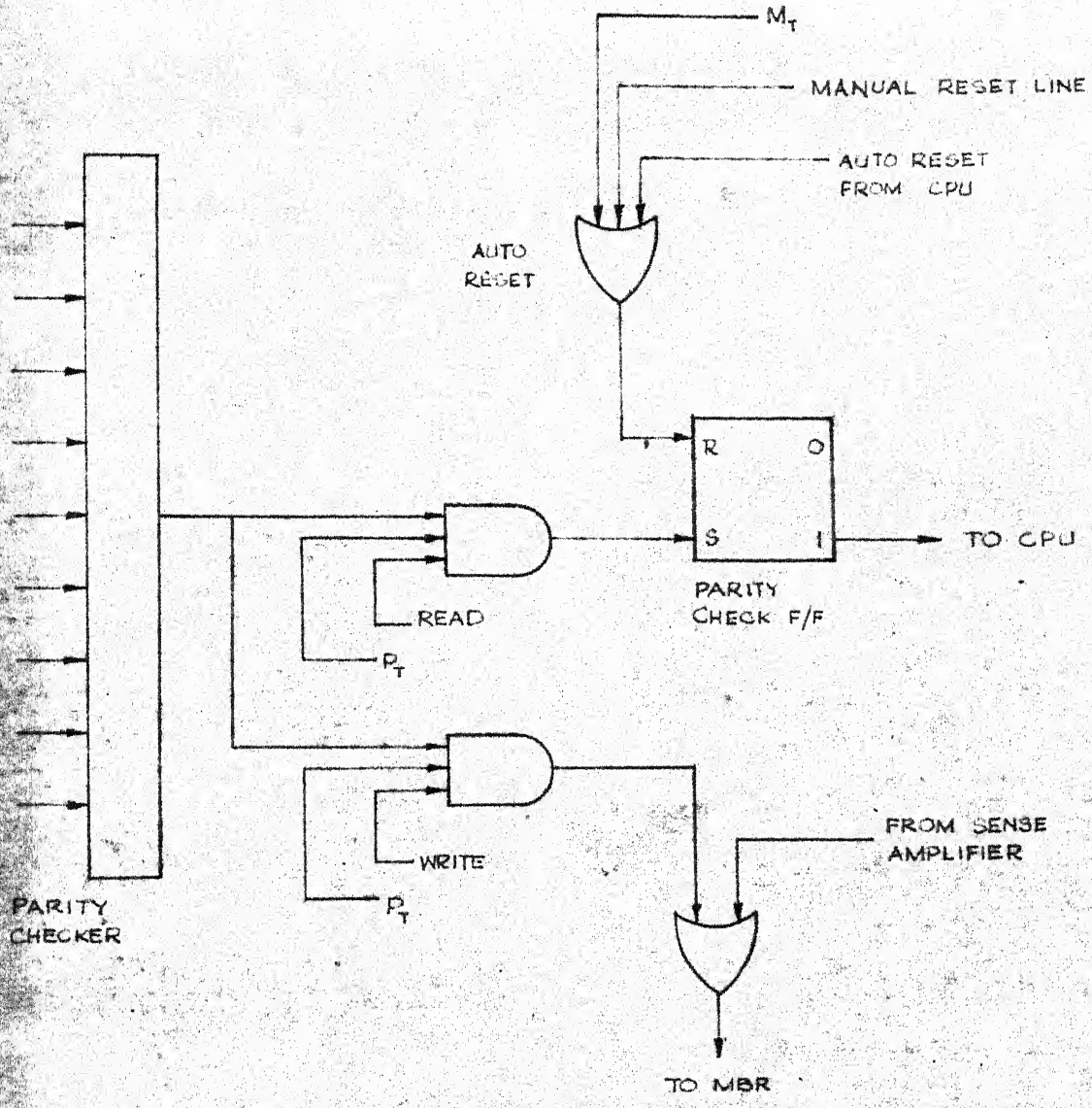


FIG 7.5 PARITY CHECK LOGIC CIRCUITRY

7.5 The Sense Amplifiers and Associated Logic Circuitry :

Fig. 7.6 shows the logic circuitry associated with the memory sense amplifiers. The inputs to the amplifiers come directly from the sense winding of the memory stack. The outputs feed the set terminals of the MBR flip flops. In the case of the sense amplifier associated with the parity check bit, the output is fed to the MBR through an OR gate. This allows the command pulse P_T to set this flip flop on the occurrence of a parity error. The gate inputs of the amplifiers are connected to a common line which is fed from a two input AND gate. In the READ/RESTORE mode, this gate routes the command pulse S_T to the gate inputs of the amplifiers. In the CLEAR/WRITE mode, S_T is blocked since this gate is inoperative. This action is necessary to prevent the information contained in the selected location from contaminating the contents of the MBR during the CLEAR operation, prior to the writing of this information into the memory. In addition, S_T is timed to occur at the instant of maximum signal to noise ratio thus ensuring reliable operation of the sense amplifiers during the READ/RESTORE mode.

7.6 The Inhibit Drivers and Associated Logic Circuitry :

The logic circuitry associated with the inhibit drivers is shown in Fig. 7.7. During the RESTORE and WRITE operations the appropriate inhibit drivers are activated when a logic '0' is to be stored in a particular bit location. Each inhibit driver is fed from a two input AND gate. When a logic '0' is to be written into a specific bit location of a word, the

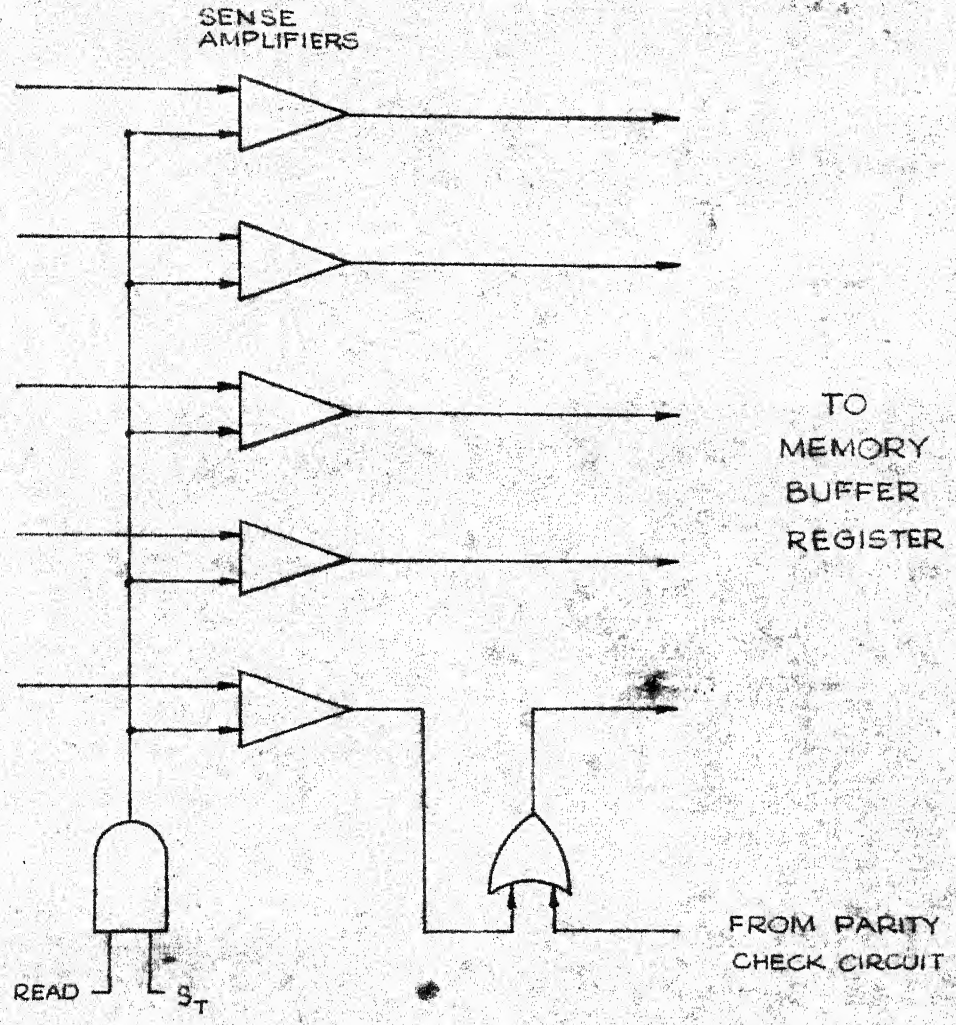


FIG 7·6 SENSE AMPLIFIER CIRCUITRY

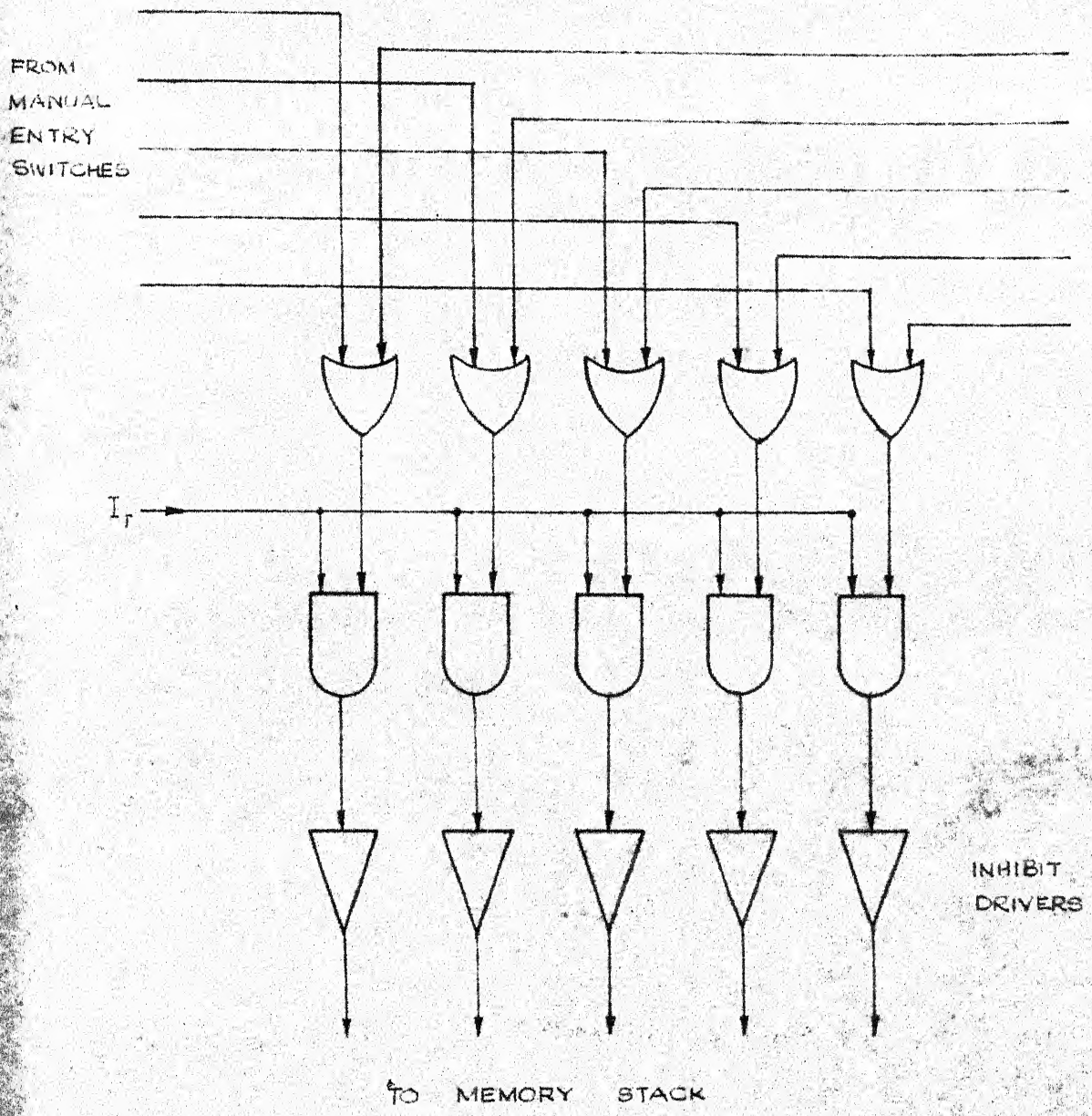


FIG 7-7 INHIBIT DRIVER LOGIC CIRCUITRY

associated flip flop of the MBR is in the reset state and consequently its logic '0' output is at a potential V. The AND gates corresponding to these flip flops are thus selected and pass the command pulse I_T to the inhibit drivers. In the locations where a logic '1' is to be written, the command pulse I_T is blocked at the AND gates.

7.7 Summary of Overall Memory Operation :

The various logic circuit blocks may be now organised as shown in Fig. 7.8 to constitute the complete CCM memory system. It can store 256 words each of length 13 bits, The aceess time is 3 microseconds and the overall cycle time is 10 microseconds.

The input lines to the memory from the CPU are :

(i) 8 address lines to the MAR.

(ii) 2 lines to the READ/WRITE circuitry.

(iii) 1 initiate line to the Timing Generator.

The output lines from the memory to the CPU are :

(i) 13 word bit lines from the MBR.

(ii) 1 parity check line from the parity check flip flop.

(iii) 1 line for the op complete signal from the Timing Generator.

In addition, reset lines from the CPU are fed to the MAR, the MBR, and the Parity check flip flop.

READ/RESTORE Operation :

At the beginning of the READ/RESTORE cycle, the CPU resets the MAR and parity check flip flop. The address of the

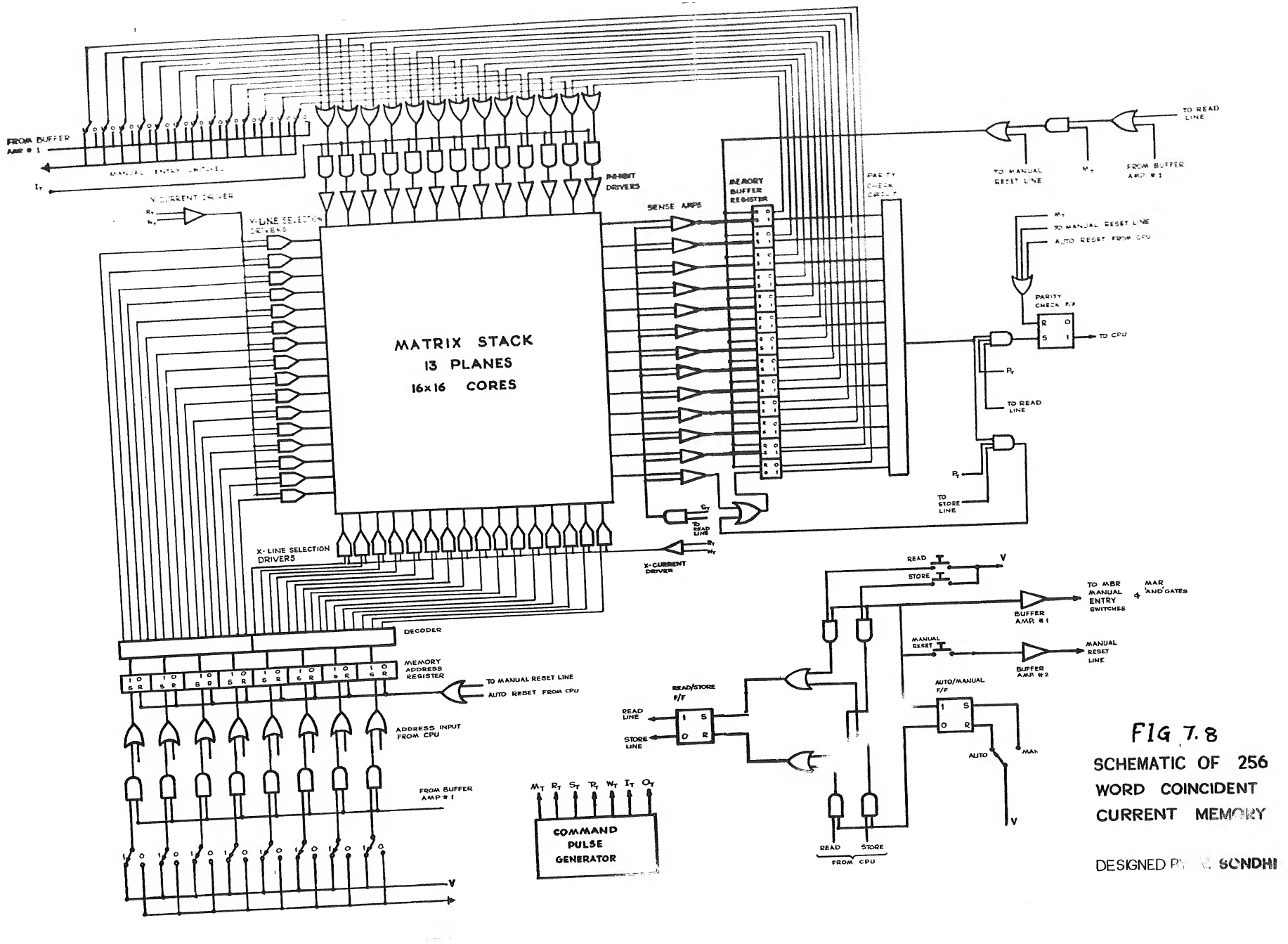


FIG 7.8

SCHEMATIC OF 256 WORD COINCIDENT CURRENT MEMORY

DESIGNED BY V. SONDHI

word to be read is stored in the MAR and the READ/RESTORE line to the READ/WRITE flip flop FF1 is energised. A 1 microsecond wide initiate pulse is sent to the Timing Generator. Command pulse M_T resets the MBR and prepares it to receive information from the sense amplifiers. This is followed by command pulse R_T which triggers the READ/WRITE current drivers. The half amplitude current pulses are routed into the selected X and Y lines by the selected line selection drivers. The cores of the selected word storing a logical '1' switch to the logical '0' state and induce a voltage on the associated sense lines. This signal is amplified by the sense amplifiers. The occurence of command pulse S_T on the gate input of the amplifiers causes the amplified signals to set the appropriate flip flops of the MBR. The parity check circuit checks the parity of the word in the MBR. If the word has odd parity, the circuit produces an output, which together with the command pulse P_T sets the parity check flip flop. If no parity error occurs the command pulse P_T is blocked at the AND gate on the input line to the parity check flip flop. The flip flops of the MBR storing a logical '0' enable the corresponding AND gates on the input lines to the Inhibit drivers. The command pulses I_T and W_T now occur simultaneously. W_T triggers the READ/WRITE current drivers. The half amplitude pulses tend to write a logical '1' in all bit positions of the selected word. However, the simultaneous occurence of I_T triggers the Inhibit drivers which generate half amplitude current pulses to counteract the effect of

the full write current in those bit locations where a logical '0' is to be written. At the termination of the command pulse I_T, the command pulse O_T is generated to signify the completion of the READ/RESTORE cycle. This pulse is routed directly to the CPU.

CLEAR/WRITE Operation :

Before the initiation of the CLEAR/WRITE cycle the word to be written into the memory is stored in the MBR. The address into which this word is to be stored is loaded into the MAR, and the CLEAR/WRITE line to the READ/WRITE flip flop FF1 is energised. The 1 microsecond initiate pulse is now sent to the Timing Generator to start the CLEAR/WRITE cycle. If the memory is in MANUAL status, the command pulse M_t clears the MBR. In this case the word to be stored is set up in the manual entry switches. In the AUTO status, M_T is blocked to prevent it from clearing the MBR. Command pulse R_T triggers the READ/WRITE current drivers. The half amplitude read pulses are routed into the selected X and Y lines through the Line selection drivers. This causes all the cores of the selected location to switch to the logical '0' state. Since the command pulse S_T is blocked at the AND gate on the gate input line to the sense amplifiers, the contents of the MBR are not contaminated. The parity of the word in the MBR is checked by the parity check circuit. If the word has even parity, no action is taken. On the other hand, if it has odd parity, the command pulse P_T in conjunction with the output of the parity check circuit sets the

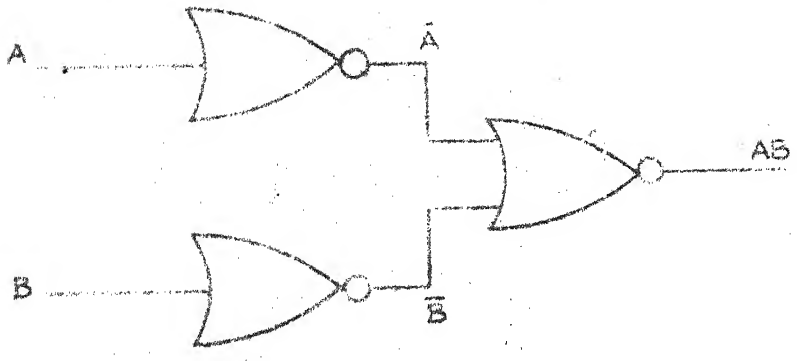
appropriate flip flop in the MBR. Hereafter, the action of the command pulses I_T and W_T is exactly the same as in the READ/RESTORE cycle and consequently the desired word is written into the specified location. Finally the command pulse O_T signals the completion of the CLEAR/ WRITE cycle.

CHAPTER VIII

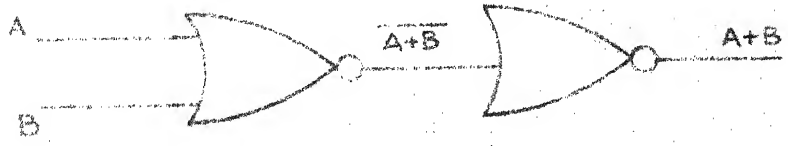
DETAILS OF CONSTRUCTION

Considering the complexity of the complete system, considerable thought must be given to the constructional details for ease of fabrication and maintenance. All circuits are made on printed circuit cards. External connections to the cards are made through 22-pin circuit connectors. The cards are mounted in bins to fit into standard 19inch racks.

Since only NOR gates were constructed it is necessary to realise the AND and OR functions using only these circuits. Fig. 8.1 shows how this can be done. However, since most outputs are obtained from flip flops, complementary outputs may be used without the need for additional inverters. Fig. 8.2 shows the realisation of the Memory Control circuitry. The wiring details are given in Fig. 8.3. The numbers associated with each block refer to the bin number, card number and pin number respectively to which a connection is made.



AND



OR

Fig. 8·1

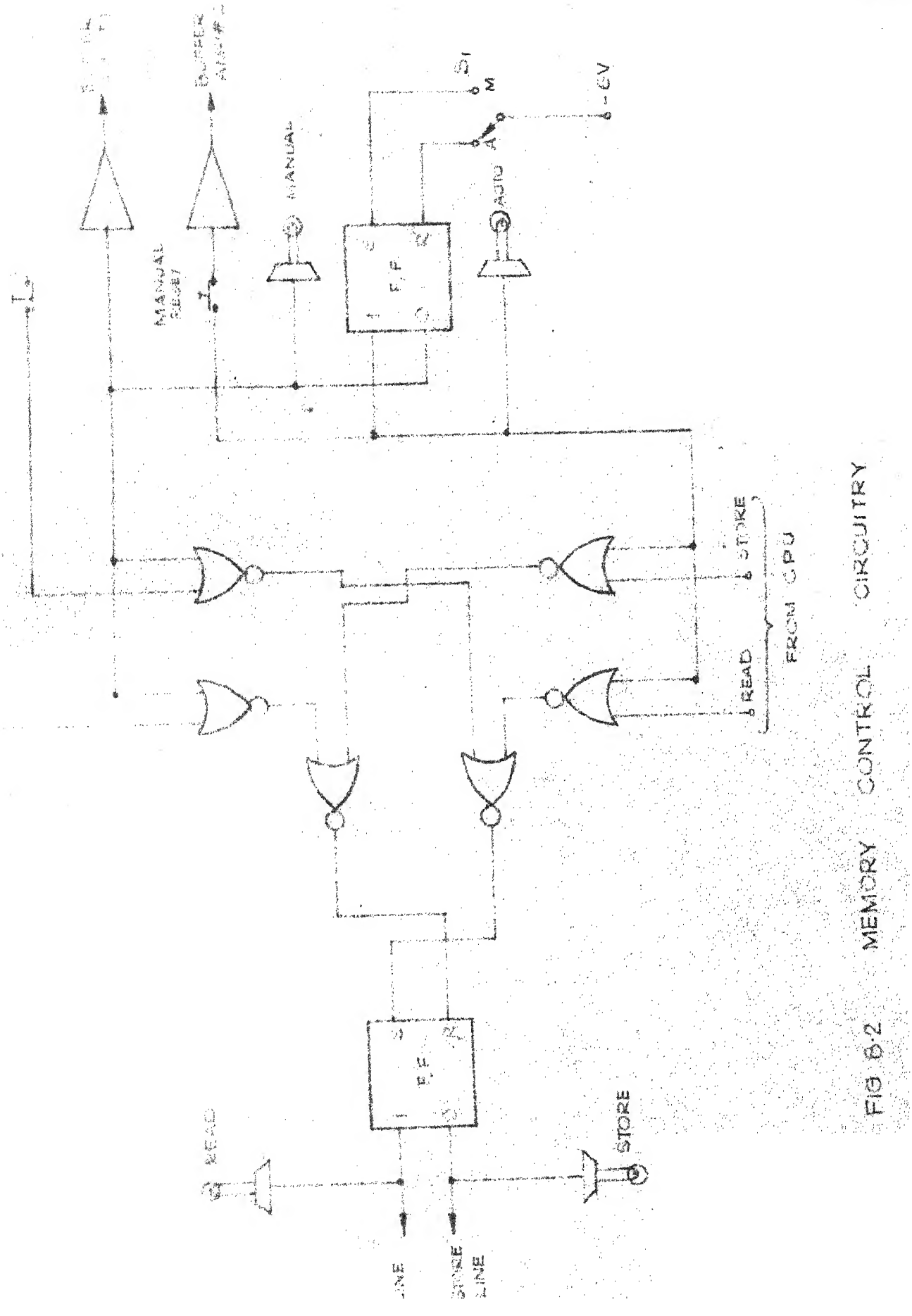


FIG 6.2 MEMORY CONTROL CIRCUITRY

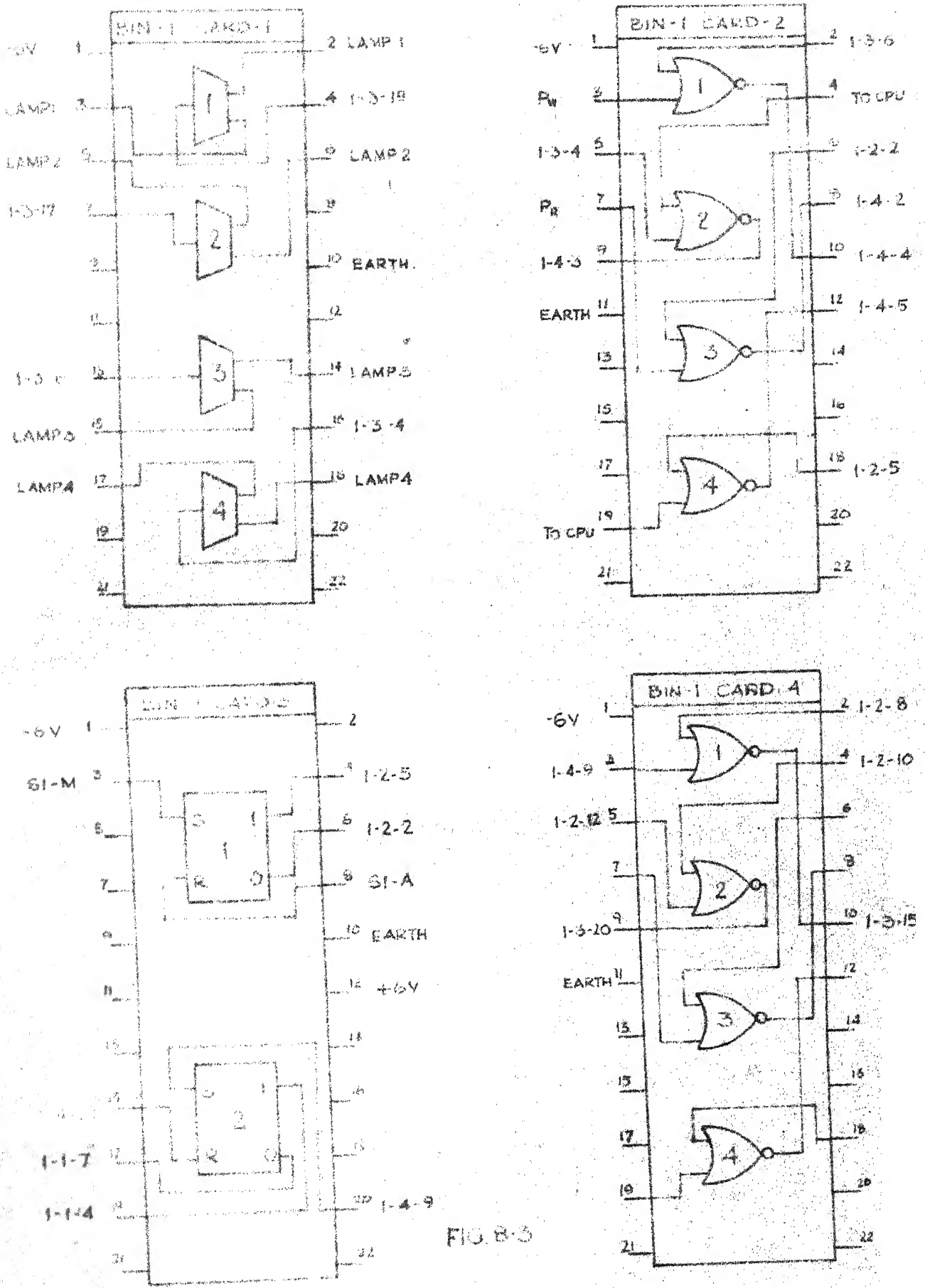


FIG. B-3

DETAILS OF MEMORY CONTROL CIRCUITRY

REFERENCES

1. Allen, C.A., Bruce, G.D., Councill, E.D., A 2.18 Microsecond Megabit Core Storage Unit, IRE Transactions on Electronic Computers, pp. 233-237, Vol. EC-10, June 1961.

2. Barker, R.C., Kmetz, A.R., Measurement of Useful Properties of Memory Devices, IRE Transactions on Magnetics, pp. 320-323, Vol. Mag-1, Dec. 1965.

3. Bartik, W.J., Bonn, T.H., A Small Coincident Current Magnetic Memory, IRE Transactions on Electronic Computers, pp. 73-78, Vol. EC-5, March 1956.

4. Best, R.L., Memory Units in the Lincoln TX-2, Proceedings of the Western Joint Computer Conference, pp. 160-167, Feb. 1957.

5. Booth, G.W., Bothwell, T.P., Logic Circuits for a Transistor Digital Computer, IRE Transactions on Electronic Computers, pp. 132-138, Vol. EC-5, Sept. 1956.

6. Christopherson, W.A., Matrix Switch and Drive Systems for a Low Cost Magnetic Core Memory, IRE Transactions on Electronic Computers, pp.238-346, Vol.EC-10, June 1961.

7. Goldstick, G.H., & Klein, E.F., Design of Memory Sense Amplifiers, IRE Transactions on Electronic Computers, pp. 236-253, Vol. EC-11, April 1962.

8. McMahon, R.E., Transistorized Core Memory, IRE Transactions on Instrumentation, pp.157-160. Vol.I-6 June 1957

9. Quartly, C.J., Square Loop Ferrite Circuitry, London, Iliffe Books, Englewood Cliffs, N.J., Prentice Hall (1962).

10. Renwick, W., Digital Storage Systems, N.Y., Wiley(1964).

11. Schwartz, S., ed., Selected Semiconductors Circuits Handbook, N.Y., Wiley (1960).

12. Siegel, P., Understanding Digital Computers, N.Y., Wiley (1961).

13. Tsui, F.F., Improving the Performance of the Sense Amplifier Through Pre-Amplification Strobing and Noise Matched Clipping, IRE Transactions on Electronic Computers, pp.677-683, Vol. EC-11, Oct. 1962.

14. Valenty, G.E., A Medium Speed Magnetic Core Memory, Proceedings of the Western Joint Computer Conference, pp. 57-67, Feb. 1957.

15. Warren, C.S., Rumble, W.G., Helbig, W.A., A Transistor Operated Magnetic Core Memory, Proceedings of the National Electronics Conference, pp.289-295, Vol.12, Oct. 1956.

16. Younker, E.J., A Transistor Driven Magnetic Core Memory, IRE Transactions of Electronic Computers, pp. 14-20, Vol EC-5, March 1957.

APPENDIX I

DESIGN OF MEMORY SENSE AMPLIFIER

Specifications :

i) Input : Bipolar pulses of minimum amplitude 50 millivolts from a transmission line of characteristic impedance 150 ohms. Risetime of the pulse is approximately 0.8 microseconds and duration 2 microseconds.

ii) Output : Unipolar pulses of minimum amplitude 6 volts and having a risetime better than 1 microsecond.

iii) Common Mode Rejection Ratio = 250.

The amplifier should have provision for strobing the output.

The complete circuit diagram is given in Fig. 5.2

Design :

The first stage of the amplifier is a difference stage.

Quiescent operating point is chosen as :

I_e = 1.5 mA per transistor

V_{cb} = -3 volts.

The bases of Q_1 and Q_2 are fed from a transmission line having a characteristic impedance of 150 ohms. Thus R_b = 150 ohms.

Allowing for a drop of 5.4 volts across R_3 or R_4 and

assuming 5% component tolerance

$1.05\ R_3 = 5.4/1.5 = 3.4$ K ohms

$R_2 = R_3$ is chosen as 3.3 K ohms

Voltage drop across R_1 or R_2 = 3 volts.

$R_1 = 3/1.5 = 2$ K ohms

$R_1 = R_2$ is chosen as 2.2 K ohms.

Capacitor C_1 effectively looks into a grounded base stage with h_{ib} = 20 ohms. For effective bypassing at 1mc/s.

$1/wC_1 = 2$ ohms.

$C = 1/(2 \times 1 \times 10^6 \times 2)$

$= 0.6$ mfd.

C_1 is chosen as 1 mfd.

Circuit Analysis :

For DC conditions the circuit may be reduced to that shown in Fig. I.1. The impedance Z seen at the first emitter is

$$Z = R_e /\!/ (h_{ib} + R_b/\beta + 1)$$

$$= h_{ib} + R_b/\beta + 1$$

$$= 20 + 150/151$$

$$= 21 \text{ ohms.}$$

Therefore input impedance is $h_{ie} = (\beta + 1)\, h_{ib}$

$= 21 \times 151$

$= 3.17$ K ohms

The input circuit of the amplifier is shown in Fig. I.2

For a 50 mv signal from a 150 ohm source, the voltage at the input terminals = 25 mv. Therefore

$$I = \frac{.025}{.150} = \frac{1}{6} \text{ mA}$$

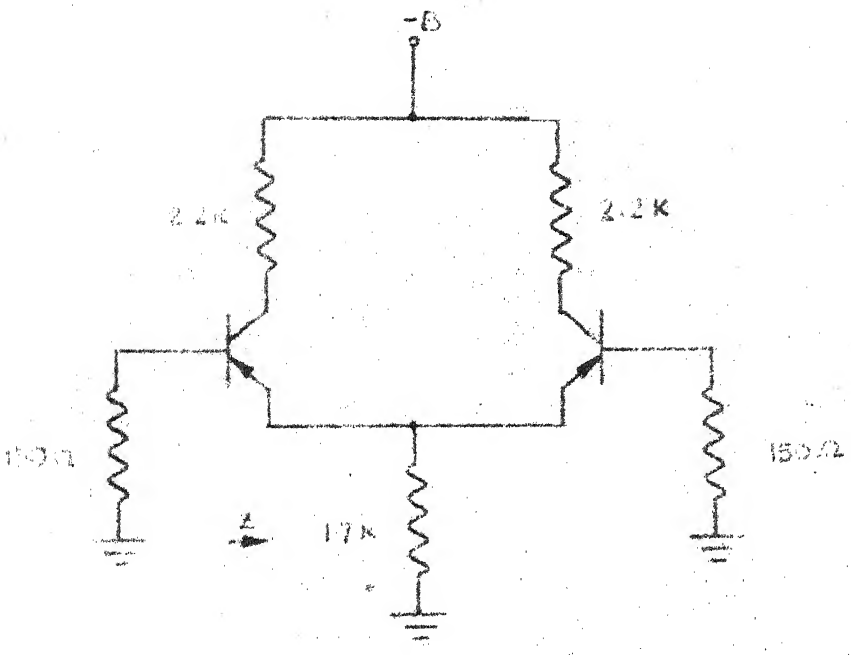


FIG. I·1

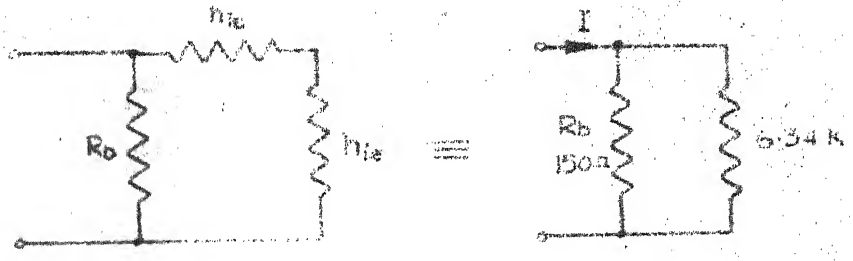


FIG. I·2

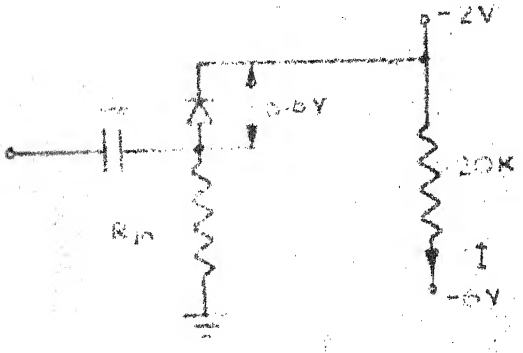


FIG. I·3

Assuming a β of 150, the collector current $= \frac{.15 \times 1 \times 150}{6.34 \times 6}$

Collector voltage swing $= \frac{.15 \times 150 \times 2.2}{6.34 \times 6} = 1.3$ volts

Therefore, voltage gain $= 1.3/.05 = 26$

Since R_b is small as compared to R_3 and R_4, the stability of the stage is approximately unity.

The second stage of the amplifier takes the bipolar signals from the first stage and produces an amplified unipolar pulse.

In the quiescent condition, RV_1 is adjusted so that the transistors Q_3 and Q_4 are cutoff. Hence only the transistor receiving a negative signal will conduct.

The load resistance R_7 may be chosen on the basis of required rise time.

For a step input to the base, the time constant for the collector current rise is given by :

$$T_r = h_{FE} (1/w_t + C_c R_7) \quad \ldots (1)$$

where

w_t = radian frequency at which current gain is unity

C_c = collector transition capacitance

h_{FE} = D.C. β

For heavy overdrive, the rise time is given by

$$t_r = 0.8 \frac{T_r \times I_{CS}}{h_{FE} \times I_B} \quad \ldots (2)$$

Where

I_{CS}/I_B = overdrive factor

From Eq. 1,

$$\frac{T_r}{h_{FE}} = (1/w_t + C_c R_7)$$

For the 2N995,

$$h_{FE} = 150$$
$$C_c = 10 \text{ pf}$$
$$f_t = 100 \text{ mc/s}$$

Therefore

$$\frac{T_r}{h_{FE}} = (1/(2 \times \pi \times 100 \times 10^6) + 10 \times 10^{-12} \times R_7)$$
$$= (.16 \times 10^{-8} + 10^{-11} \times R_7)$$

Substitute in Eq.2 and find R_7 for the required rise time. For a rise time of 0.3 microseconds, and base overdrive of 10 times, $0.3 \times 10^{-6} = 0.8 \times 10 \times (.16 \times 10^{-8} + 10^{-11} \times R_7)$

$$R_7 = 3.59 \text{ K ohms}$$

R_7 is chosen as 3.3 K ohms.

For saturation, voltage drop across R_7 = 3 volts

Therefore collector current = 3/3.3 = 0.91 ma

Base current with 10 times overdrive = 10 x .91/150 = 0.0606 ma

With the threshold level adjusted so that Q_3 and Q_4 are just cutoff, voltage drop across R_5 or R_6 = 1.3 volts

Therefore $R_5 = 1.3/.06 = 21.6$ K ohms.

Choose $R_5 = R_6$ as 22 K ohms.

Capacitor C_4 may be chosen for a 10% tilt on the output

$$P = \frac{(h_{fe} + 1) \ t}{RC} \times 100\%$$

Where :

$R = R_s + h_{ie}$

R_s = Source resistance

h_{ie} = 3 K ohms for 2N995

t = pulse width

Therefore for a pulse width of 2 microseconds and R_s = 22 K,

$$C_4 = \frac{151 \times 2 \times 10^{-6} \times 100}{25 \times 1000} = .121 \text{ mf}$$

Choose C_4 as 0.1 mf

The speed up capacitors C_2 and C_3 are chosen experimentally for best rise and fall time.

The output circuit of the amplifier is required to have provisions for strobing. On considerations of rise time, R_8 is selected as 3.3 K ohms. With no pulse input at either terminal, the emitter is at -6 volts and the base is required to be at -2 volts. Collector current required to saturate Q_5 when the input rises to - 3 volts and D_1 is cut-off = 6/3.3. = 1.8 ma

Therefore base current with 10 times overdrive

$$= \frac{1.8 \times 10}{150} = 0.12 \text{ ma}$$

Voltage drop across R_9 = 6 - 3.6 = 2.4 volts

Therefore R_9 = 2.4/0.12 = 20 K ohms

When D_1 is conducting, the base must be at -2 volts. The circuit condition is given in Fig. I.3

$$I = 4/20 = 0.2 \text{ ma}$$

Therefore $R_{10} = \frac{2 - 0.6}{0.2} = 7$ K ohms

Choose R_{10} as 6.8 K ohms. C_5 is chosen for best rise time Capacitor C_6 with R_{10} should have a time constant greater than 1 microsecond,

For a time constant of 50 microseconds,

$$C_1 R_2 = 50 \times 10^{-6}$$

$$C_1 = \frac{50 \times 10^{-6}}{6.8 \times 10^{3}} = 0.00735$$

C_1 is chosen as 0.01 mfd

The complete circuit diagram of the amplifier is given in Fig. 5.2

APPENDIX II

DESIGN OF CURRENT DRIVER AMPLIFIERS

Specifications :

The current driver amplifiers are required to supply current pulses of -400 milliamps and +400 milliamps into a 10 ohms load. The pulse rise time is required to be less than 0.5 microseconds with a duration of 3 microseconds. The amplifiers are driven by +6 and -6 volt pulses of 3 microseconds duration and having a maximum drive capability of 5 milliamps.

Design :

The complete circuit diagram is given in Fig. 5.4

The Positive Current Driver

When Q_3 is conducting 400 milliamps,

$$.4 \times R_6 + .4 \times 12 + V_{ce}\ \text{sat.} = 12$$

$$V_{ce}\ \text{sat} = 1\ \text{volt}$$

$$\text{Therefore } R_6 = 6.2/.4 = 15.5$$

R_6 is chosen as 15 ohms

Assuming a β of 20 for Q_3, base current = 400/20 = 20 ma

The circuit condition when Q_2 is conducting is shown in Fig. II.1

Voltage drop across R_5 = 5.4 - 3.5 = 1.9 volts

Therefore R_5 = 1.9/.02 = 95 ohms.

R_5 is chosen as 100 ohms.

When Q_2 switches on, its collector current rises with a time constant given by :

$$T_r = h_{FE}\ (1/w_t + C_c\ R_4)$$

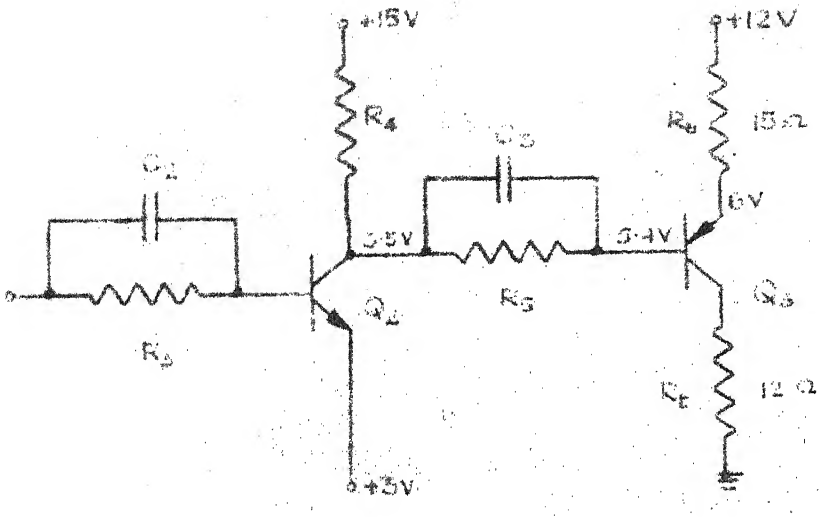


FIG II·1

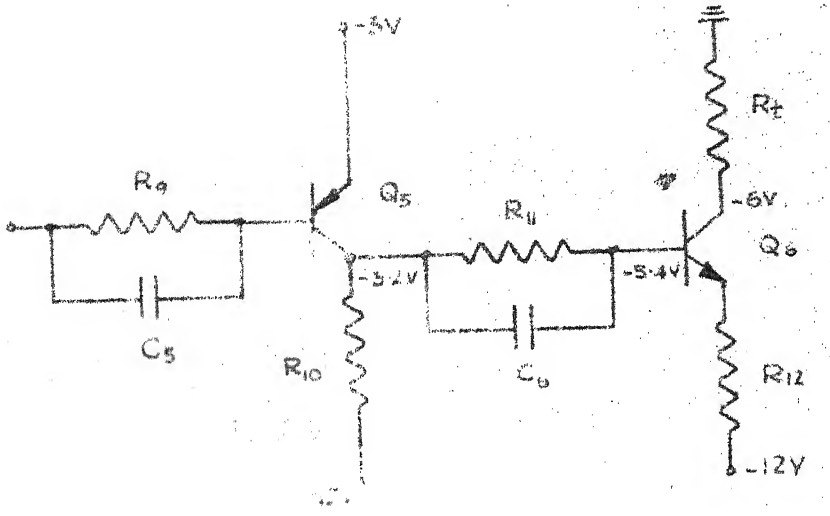


FIG II·2

Where

h_{FE} = D.C. β

w_t = radian frequency at which current gain is unity

C_c = Collector transition capacitance

For the CIL 511,

$h_{FE} = 50$, $w_t = 100$ mc/s, $C_c = 25$ pf

$$T_r/h_{FE} = 1/(2\pi \times 100 \times 10^6) + 25 \times 10^{-12} \times R_4$$

$$= .16 \times 10^{-8} + 25 \times 10^{-12} \times R_4$$

With base overdrive of 10 times, the rise time is given by :

$$t_r = 0.8 \times \frac{T_r}{h_{FE}} \times \frac{I_{cs}}{I_b}$$

Where I_{cs}/I_b is the base overdrive factor = 10

For a rise time of 0.5 microseconds, therefore,

$$0.5 \times 10^{-6} = 0.8 \times 10 \times (0.16 \times 10^{-8} + 25 \times 10^{-12} \times R_4)$$

$$R_4 = 2.44$$

R_4 is chosen as 2.2 K ohms

Total emitter current of $Q_2 = \frac{15 - 3 - 0.5}{2.2} + 20 = 25.2$ ma

Assuming a β of 50, the base current of $Q_2 = 25.2/50$

$= 0.5$ ma

With base overdrive of 10 times, the base current = 5 ma

When Q_1 is cutoff, the voltage drop across R_2

and $R_3 = 12 - 3 - 0.6 = 8.4$ volts

Therefore $R_2 + R_3 = 8.4/5 = 1.68$ K ohms.

Choosing $R_2 = R_3 = 820$ ohms

When Q_1 is conducting, the collector current required to saturate it $= 12 - V_{ce}sat/ .82 = 11.5/.82 = 14$ ma

Therefore base current $= 14/50 = 0.28$ ma

$$R_1 = \frac{12 - 0.6}{0.28} = 40.6$$

R_1 is chosen as 39 K ohms.

C_1 with R_1 should have a time constant greater than 3 microseconds. For a time constant of 50 microseconds,

$$R_1 C_1 = 50 \times 10^{-6}$$

$$C_1 = \frac{50 \times 10^{-6}}{39 \times 10^{3}}$$

$$= 1.28 \times 10^{-9}$$

Choose C_1 as .001mfd

The Negative Current Driver

As with the positive current driver, $R_{12} = 15$ ohms

Assuming a β of 20 for Q_6, base current $= 400/20 = 20$ ma

Circuit condition when Q_5 is conducting, Voltage drop across $R_{11} = 5.4 - 3.2 = 2.2$ volts

Therefore $R_{11} = 2.2/.02 = 110$ ohms.

R_{11} is chosen as 100 ohms.

When Q_5 switches on the time constant of the collector current rise is ,

$$T_r = h_{FE} (1/w_t + C_c R_{10})$$

For the 2N995 :

$h_{FE} = 90$, $w_t = 100$ mc/s, $C_c = 10$ pf

$$T_r/h_{FE} = 1/(2\pi \times 100 \times 10^{6}) + 10 \times 10^{-12} \times R_{10}$$

$$= .16 \times 10^{-8} + 10 \times 10^{-12}$$

With base overdrive of 10 times, the rise time is given by :

$$t_r = 0.8 \times \frac{T_r}{h_{FE}} \times \frac{I_{cs}}{I_b}$$

For a rise time of 0.5 microseconds, therefore,

$$0.5 \times 10^{-6} = 0.8 \times 10 \times (0.16 \times 10^{-8} + 10 \times 10^{-12} \times R_{10})$$

$$R_{10} = 6.09$$

R_{10} is chosen as 5.6 K ohms.

Total emitter current of $Q_5 = \frac{15 - 3 - 0.2}{5.6} + 20 = 22.1$ ma

Assuming a β of 90, the base current of $Q_5 = 22.1/90 = 0.25$

With base overdrive of 10 times, base current = 2.5 ma

When Q_4 is cutoff, voltage drop across R_8 and R_9 = 12-3-0.6

Therefore $R_8 + R_9 = 8.4/2.5 = 3.36$

Choosing $R_8 = R_9 = 1.5$ K ohms.

When Q_4 is conducting, the collector current required to saturate it $= \frac{12 - V_{ce}sat}{1.5} = \frac{11.8}{1.5} = 7.86$ ma

Therefore base current $= 7.86/90 = .088$ ma

$$R_7 = 12 - 0.6 / 0.088 = 130$$

R_7 is chosen as 120 K ohms.

C_4 with R_7 should have a time constant greater than 3 microseconds. For a time constant of 50 microseconds,

$$R_7 C_4 = 50 \times 10^{-6}, \quad C_4 = \frac{50 \times 10^{-6}}{120 \times 10^3}$$

$$= .416 \times 10^{-9}, \quad C_4 = 470 \text{ pf.}$$

The Positive Current Driver is also used to perform the Inhibit function.

APPENDIX III

DESIGN OF LINE SELECTION DRIVERS

Specifications :

The line selection drivers are required to pass current pulses of - 400 ma and + 400 ma when selected by a level of -6 volts. When not selected, they are required to block both polarities of current.

The complete circuit diagram is given in Fig. 5.6

Design :

When Q_1 is turned on, the circuit condition is, shown in Fig. III.1.

Assuming a β of 20, the base current of Q_1 = 20 ma

Voltage drop across R_1 = 10.9 - 5.2 = 5.7 volts

$$R_1 = 5.7/0.02 = 285$$

Choose R_1 as 250 ohms

When Q_2 switches on, the collector current rise time is determined by R_2. From Appendix II, R_2 is chosen as 2.2 K ohms. Total emitter current of $Q_2 = \frac{12 + 11.5}{2.2} + 20$

$$= 30.7 \text{ ma}$$

Therefore, base current = 30.7/50 = 0.615

The circuit condition when Q_2 and Q_3 conduct is shown in Fig. III.2.

Voltage drop across R_3 = 11.4 - 0.2

Base current of Q_2 with 10 times overdrive = 6.15 ma.

Therefore R_3 = 11.2/6.15 = 1.82

R_3 is chosen as 1.8 K ohms.

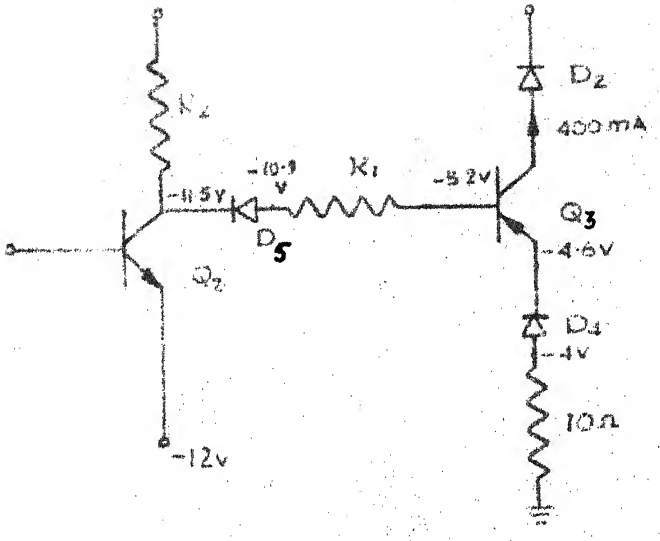


FIG III·1

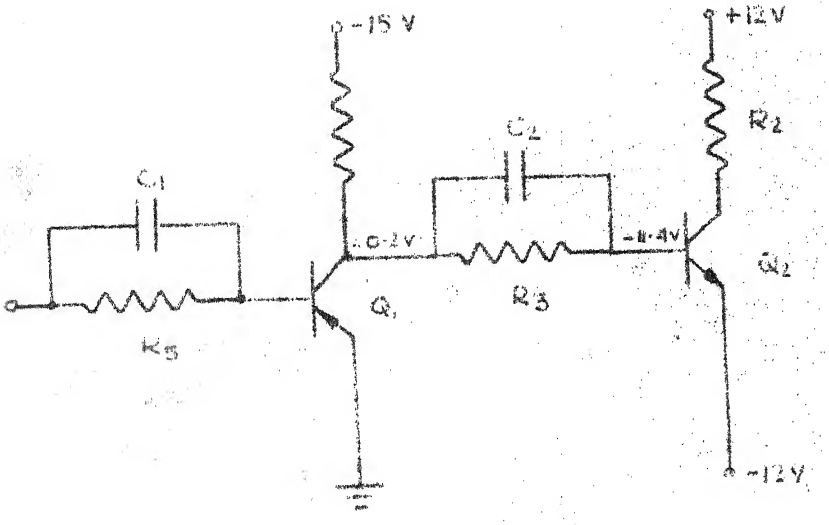


FIG III·2

R_4 is chosen on the basis of required rise time as 5.6 K ohms. Collector current required to saturate

$$Q_3 = \frac{15 - 0.2}{5.6} = 2.64 \text{ ma}$$

Total emitter current of

$$Q_3 = 2.64 + 6.15 = 8.79 \text{ ma}$$

Therefore base current

$$= 8.79/90 = 0.0976$$

With overdrive, base current

$$= 1.0 \text{ ma}$$

Therefore $R_5 = \frac{6 - 0.6}{1.0} = 5.4$

R_5 is chosen as 5.6 K ohms

The speed up capacitors are chosen experimentally.

APPENDIX IV

DESIGN OF AND GATE

Specifications :

(i) Number of inputs is 4

(ii) Rise time should be 0.5 microseconds or better

(iii) Voltage corresponding to the Boolean variables are :

'1' -6 V

'0' 0 V

(iv) Maximum drive capability 5 ma

The circuit diagram is given in Fig. 5.10

Design :

The design consists of choosing a value for the supply voltage V, and the resistance R_1 for the required rise time and allowable dissipation in R_1.

A compromise between rise time and the ratio P_1 / P_d, where P_1 = maximum power that can be delivered to the load.

P_d = power dissipated in R_1

leads to the following relations,

$$V = 4E$$

$$R_1 = 3t_r/C$$

Where :

E = voltage corresponding to the Boolean '1'

t_r = required rise time

C = diode capacitance + stray capacitance

Assuming 5% component tolerance and 10% supply voltage

variation $V_{min} = 4E_{max}$

$R_1 \text{ max} = 3t_r / C \text{ max}$

Assuming C max = 100 pf

$V_{min} = 4 \times -6.6 =$

$= -26.4$

Therefore the nominal value of

$V = -(26.4 + 2.64)$

$= -29.4$

V is selected as 30 volts.

For a rise time of 0.1 microseconds,

$$R_1 \text{ max} = \frac{3 \times 0.1 \times 10^{-6}}{100 \times 10^{-12}}$$

$= 3$ K ohms.

Therefore the nominal value of R_1 is taken as:

$= 3 - 0.3$

$= 2.7$ K

Maximum load current that the gate can supply :

$$= \frac{30 \div 6}{2.7}$$

$= 9$ ma

APPENDIX V

THE PARITY CHECK CIRCUIT

The basic circuit used in the Parity checker is shown in Fig. 5.12 This circuit may be conveniently constructed by modifying the two input TRL NOR circuit. This modification is shown in Fig. V.1.

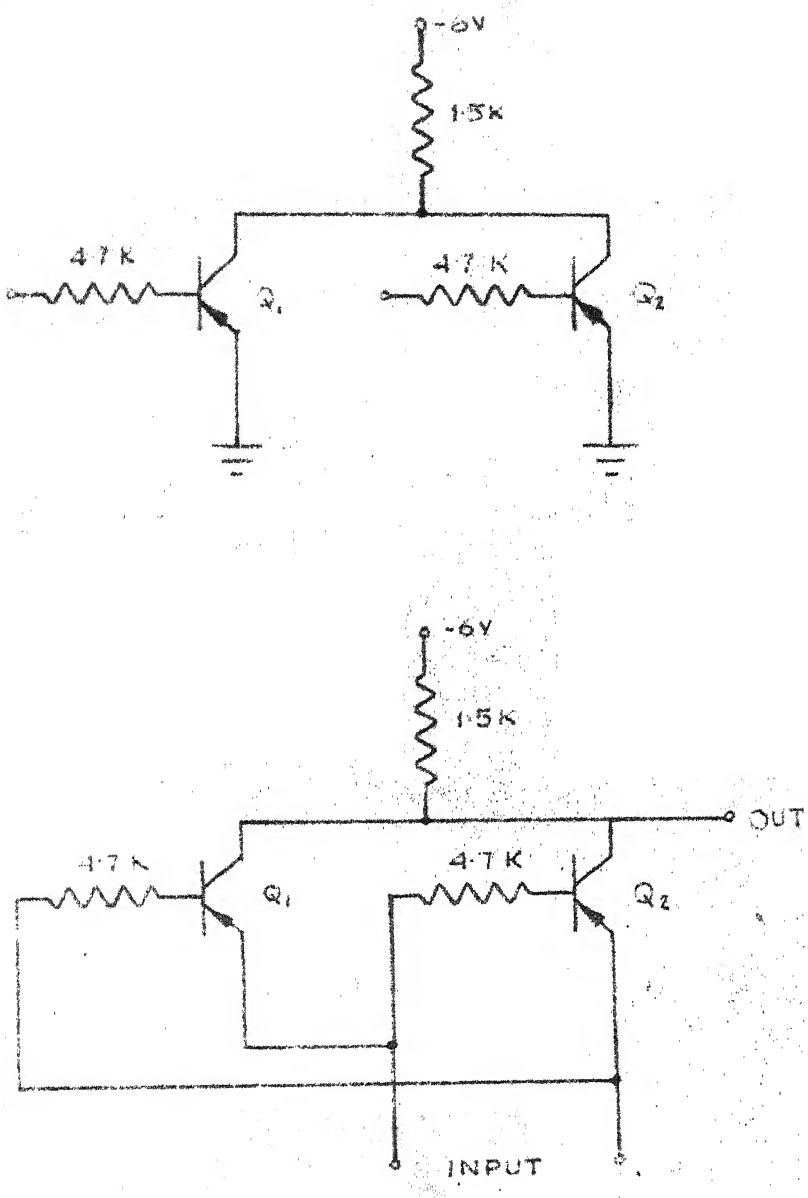


FIG. V-1